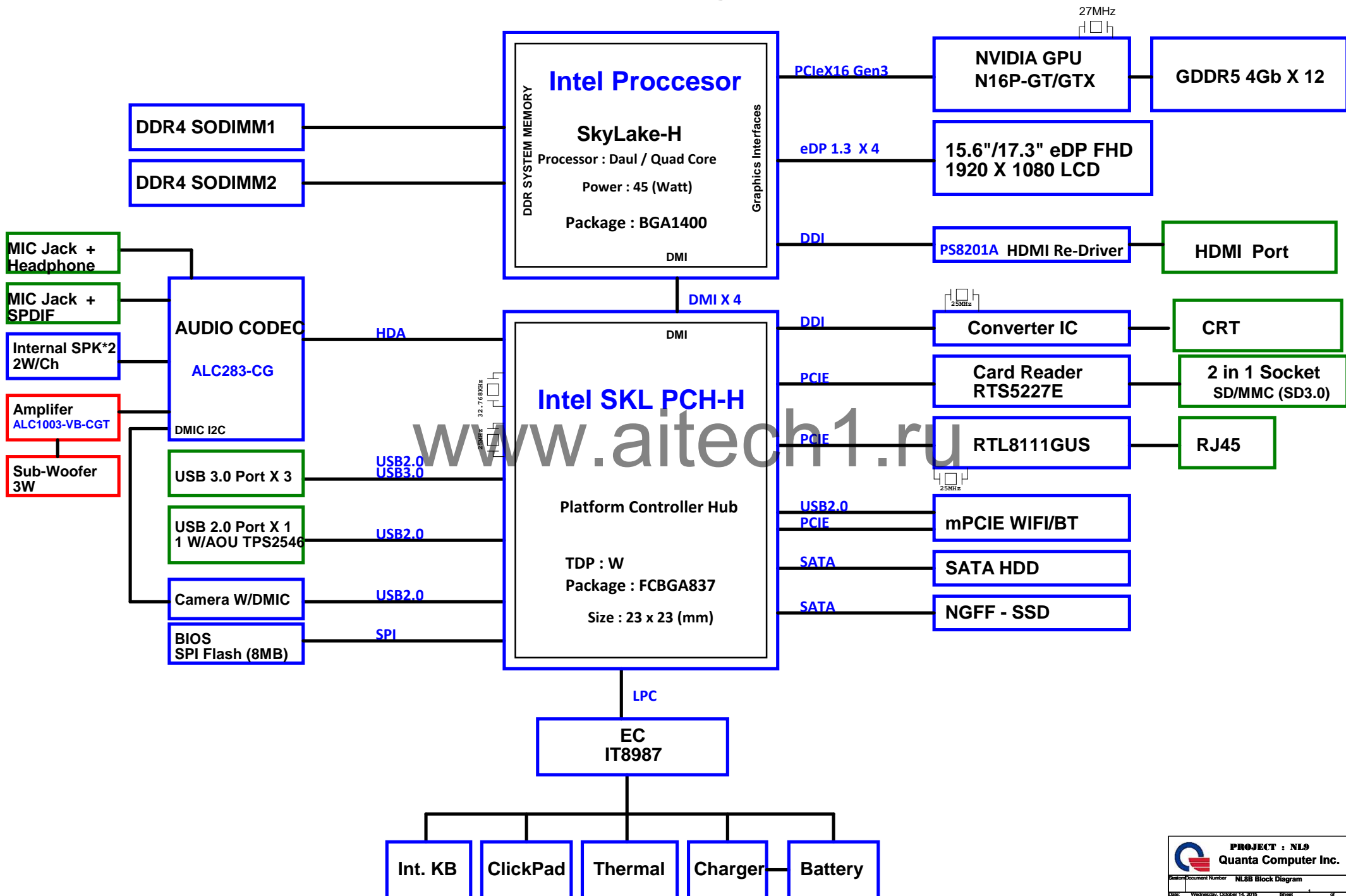


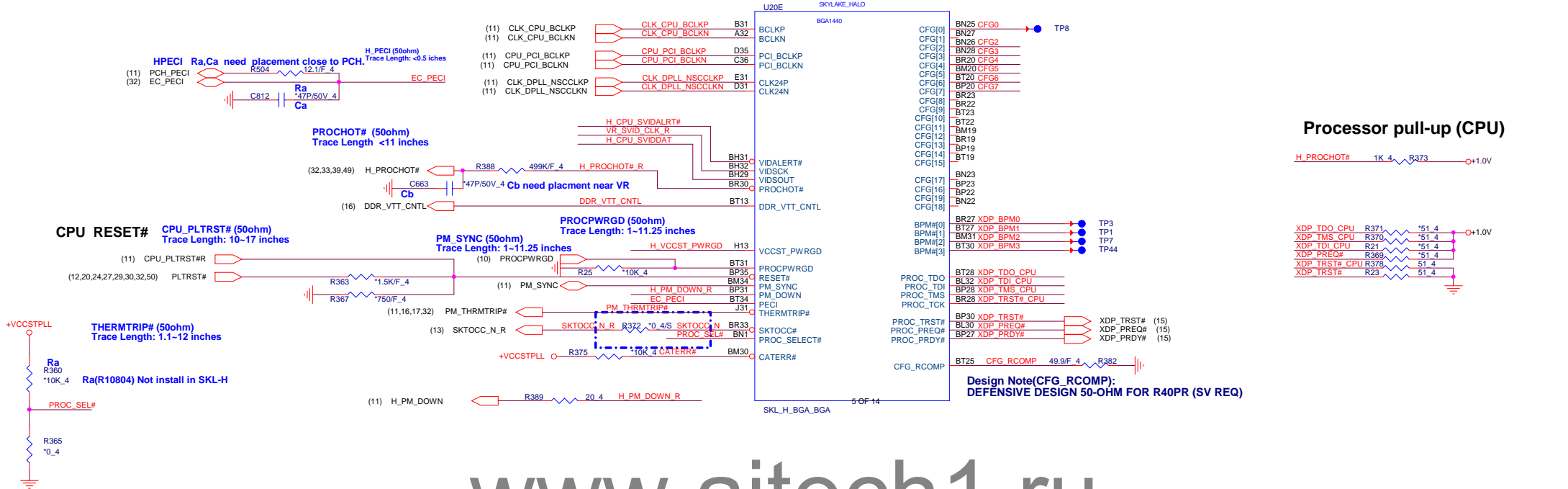
# NL9 Block Diagram

01

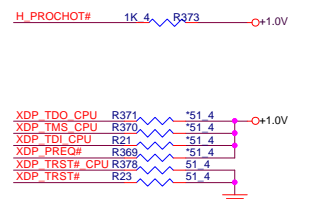


# SKYLAKE Processor (CLK,MISC,JTAG)

Host CLK:  
Trace length < 11000 MILS  
Trace spacing = 15, 20 MILS, Impedence 90 ohm



## Processor pull-up (CPU)



Design Note(CFG\_RCOMP):  
DEFENSIVE DESIGN 50-OHM FOR R40PR (SV REQ)

## CPU CORE SVID

Layout note: need routing together and ALERT need between CLK and DATA.

CLOSE TO CPU  
PLACE THE PU RESISTORS



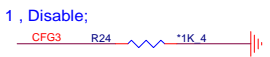
PLACE THE PU RESISTORS  
CLOSE TO VR  
PULL UP IS IN THE VR MODULE



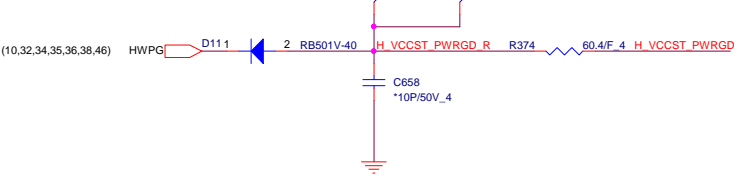
CLOSE TO CPU  
PLACE THE PU RESISTORS



0 Enable; SET DFX ENABLED BIT IN DEBUG

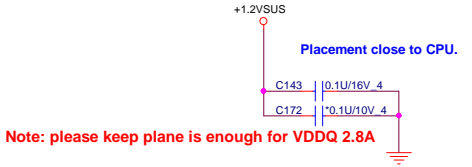


R10479 close to CPU side  
H\_VCCST\_PWRGD trace 0.3" - 1.5"



Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	Note that some of the Intel reference designs board might connect CFG[0] to HOOK[2]. This route is not needed on a Oxm board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	CFG2 R26 1K 4
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	CFG4 R385 1K 4
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	CFG6 R390 1K 4 CFG5 R379 1K 4
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asserted x0 = PEG wait for BIOS fro training	CFG7 R384 1K 4

## CPU VDDQ

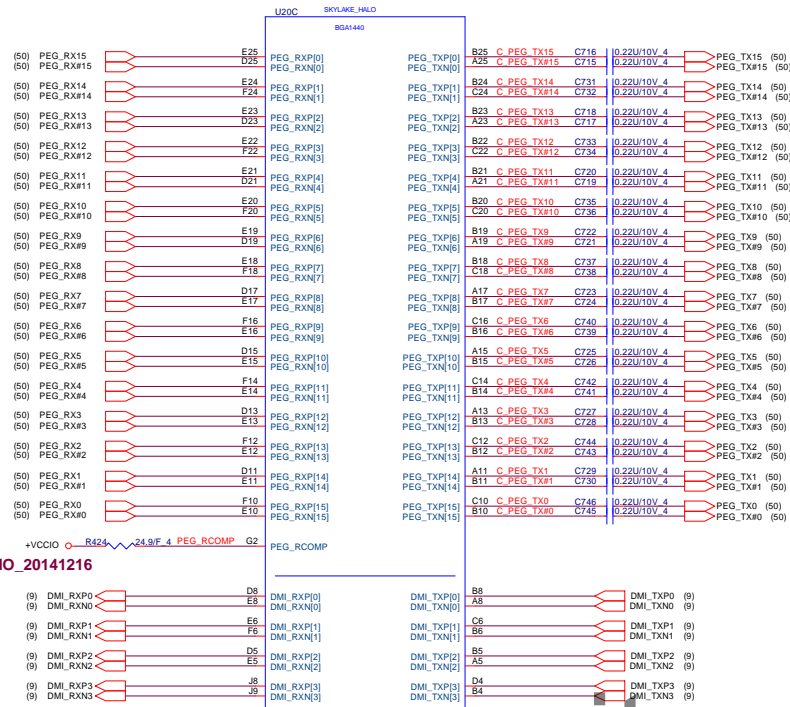


Note: please keep plane is enough for VDDQ 2.8A

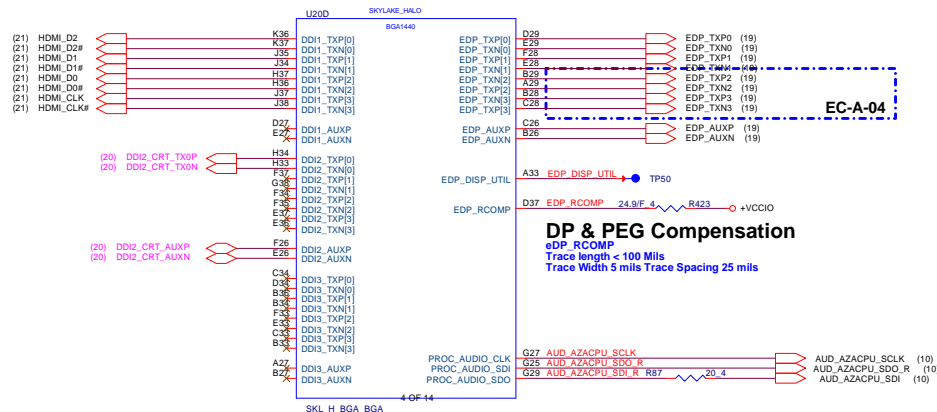
**PROJECT : NL9**  
**Quanta Computer Inc.**

Size	Document Number	02 - SKYPAKE 1/20(eDP/DDI)	Rev	1A
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PEG\_RCOMP  
Trace length < 400 MILS  
Trace width = 5 MILS  
Trace spacing = 15 MILS  
Change PWR rail from +1.0V to +VCCIO\_20141216

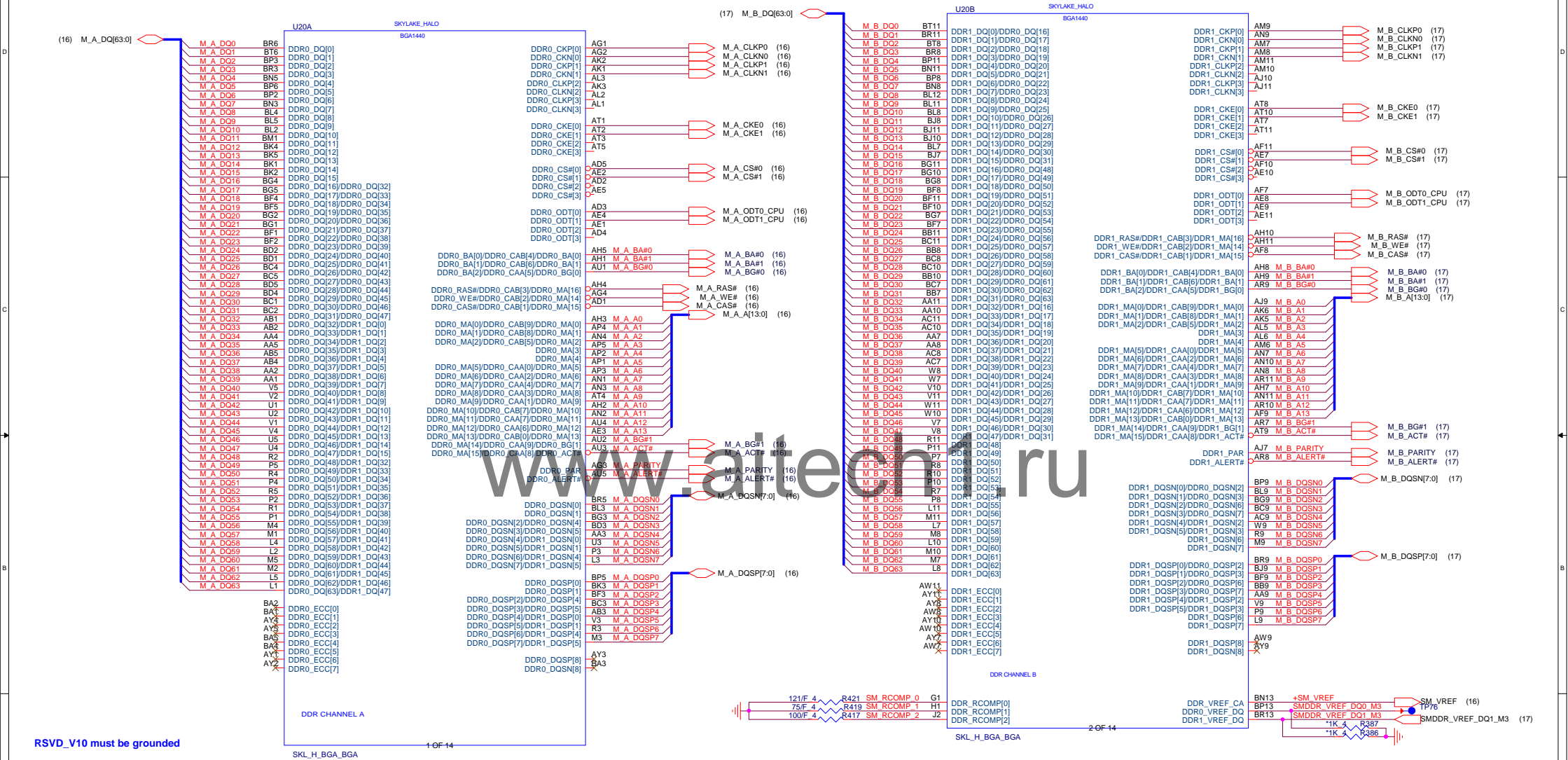


CRT



+VCCIO (6.37)  
+1.2VSBUS (2.6,10,16,17,35,44,47)  
+3V\_S5 (10,12,14,18,24,27,31,32,34,35,37)  
+3V (8,10,11,12,13,14,16,17,19,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42,43,44,45,46,47,48,49,50,51,52,53,54,55,56,57,58,59,60,61,62,63,64,65,66,67,68,69,70,71,72,73,74,75,76,77,78,79,80,81,82,83,84,85,86,87,88,89,90,91,92,93,94,95,96,97,98,99,100)

## SKYLAKE Processor (DDR3)





Follow SKL H EDS page 133 to 45W(GT4+OPC): +VCCGT=104A/12A (GTx)  
Follow SKL H EDS page 133 to 45W(GT2): +VCCGT=55A

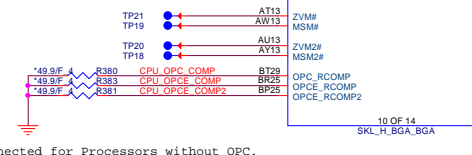
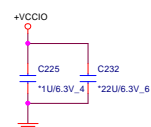
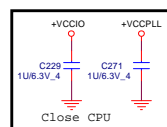
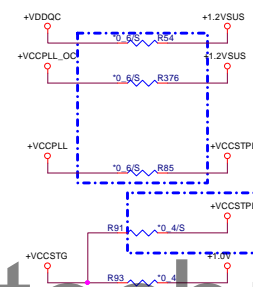
+VCC CORE (7,40,44)  
+1.2VSSUS (2,6,10,16,17,35,44,47)

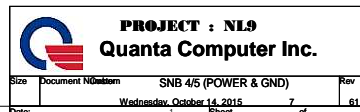
4+4e, Support eDRAM Only, GTX 12A



VCCGT\_SENSE (39)  
VSSGT\_SENSE (39)  
VSSGT\_SENSE (39)  
VSSGT\_SENSE (39)

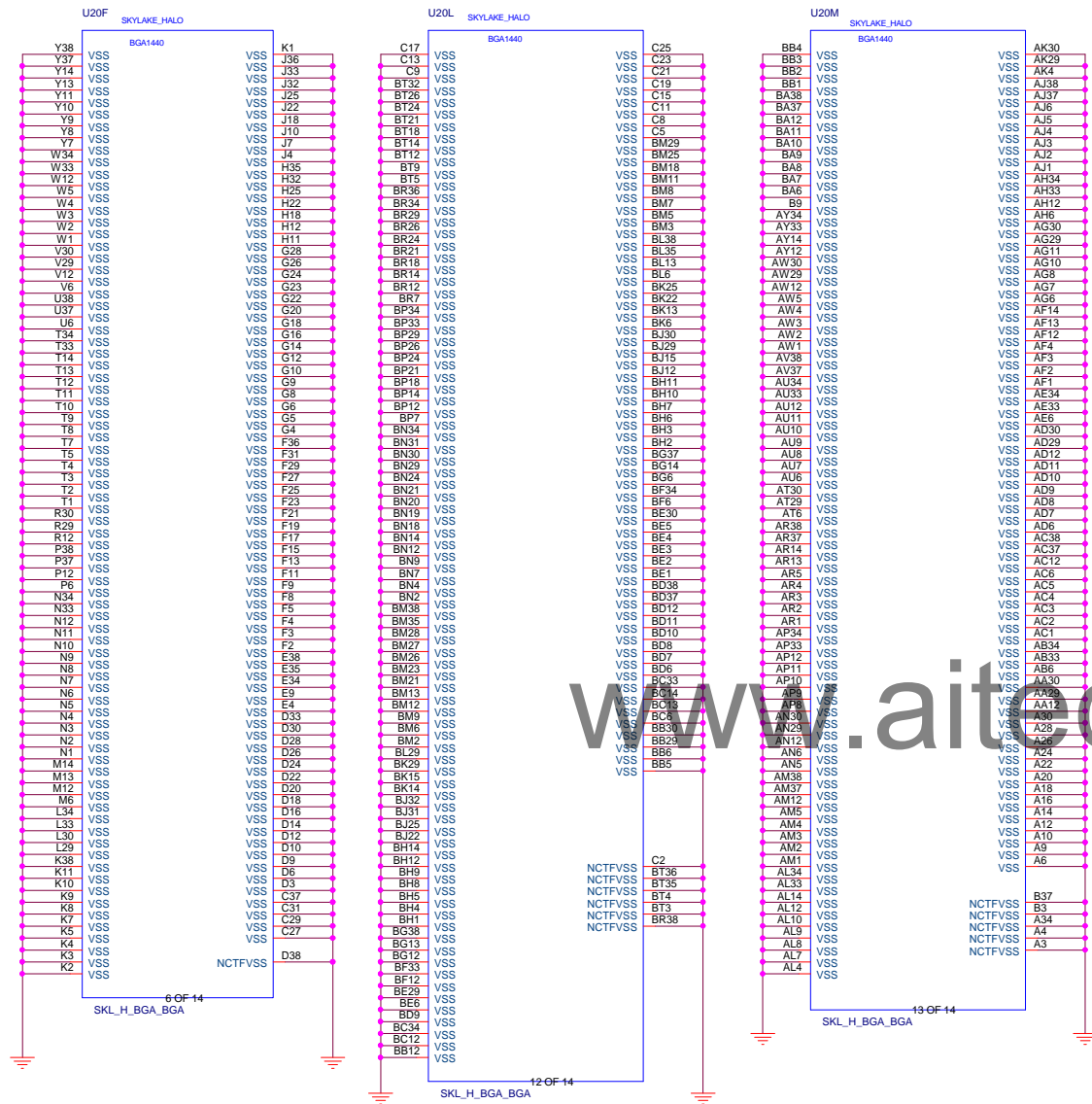
VCC Output Decoupling Recommendations

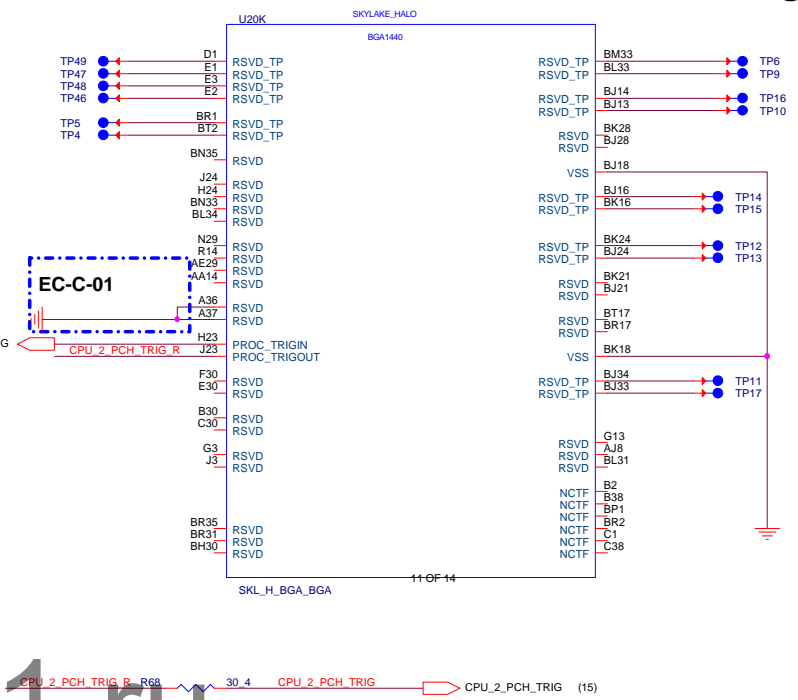


# Haswell Processor (GND)

# Haswell Processor (RESERVED, CFG)



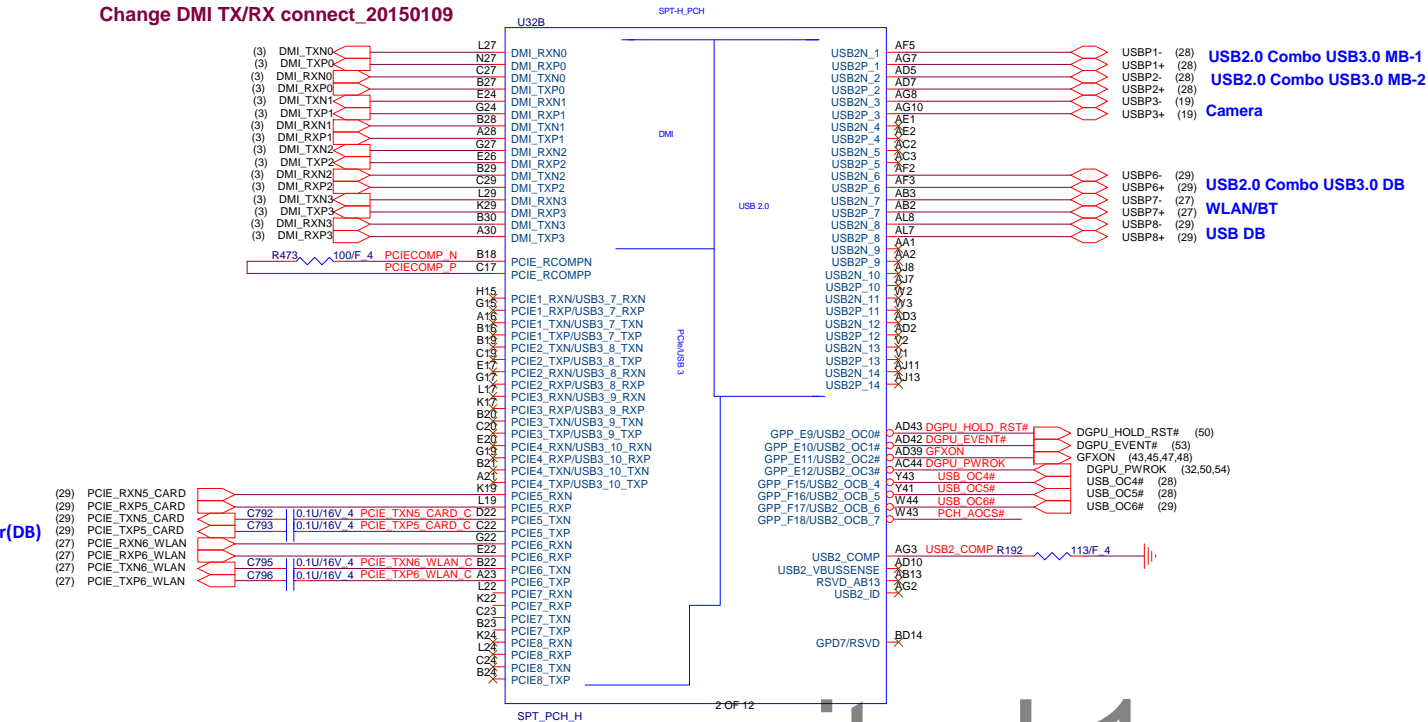
www.aitech1.ru



## Change DMI TX/RX connect\_20150109

Cardreader(DB)

WLAN



## GPU Strap

DFX TEST MODE  
XTAL INPUT IS SINGLE ENDED IF  
SAMPLED LOW ELSE DIFFERENTIAL

DGPU\_PWROK \*10K 4 R496

## RING OSCILLATOR BYPASS

DGPU\_HOLD\_RST# \*10K 4 R502

## XTAL INPUT FREQUENCY[0]

DGPU\_EVENT# \*100K 4 R498

## XTAL INPUT FREQUENCY[1]

GFXON \*10K 4 R190

## DGPU\_EVENT#-- For BIOS check

DGPU\_EVENT# \*10K 4 R497

DGPU\_HOLD\_RST# \*10K 4 R501

GFXON \*10K 4 R193

DGPU\_PWROK \*10K 4 R495

SIO\_EXT\_SMI# \*10K 4 R489

EC\_RCIN# \*10K 4 R249

USB\_OC4# \*10K 4 R494

USB\_OC5# \*10K 4 R491

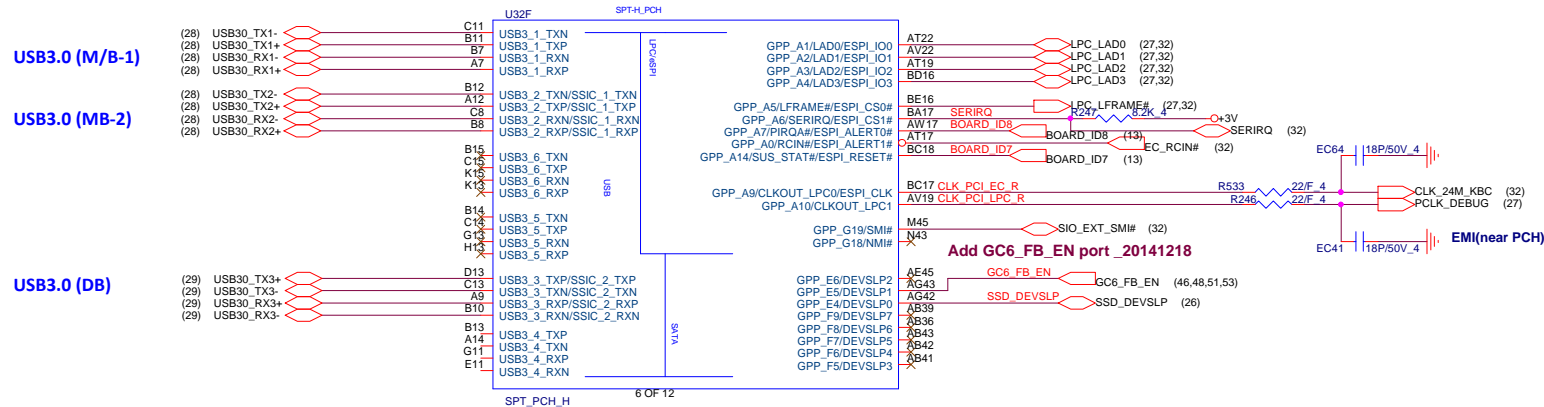
USB\_OC6# \*10K 4 R493

PCH\_AOCS# \*10K 4 R492

USB3.0 (M/B-1)

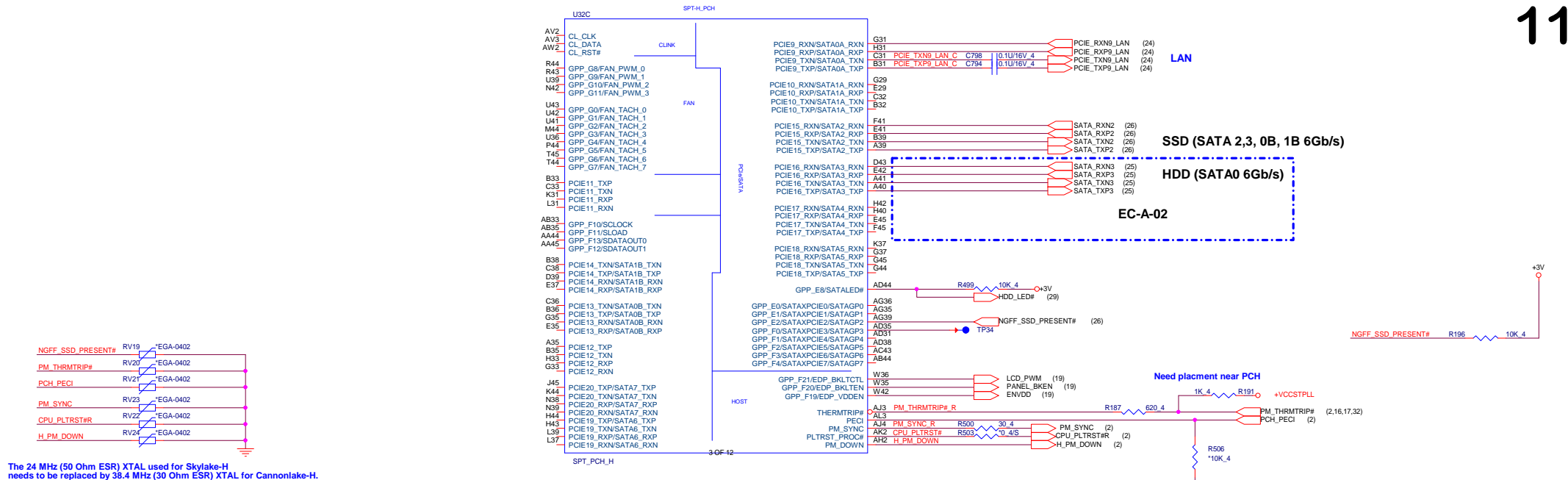
USB3.0 (MB-2)

USB3.0 (DB)

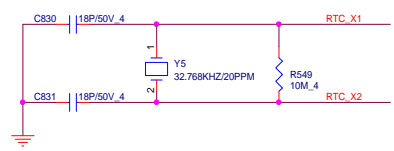


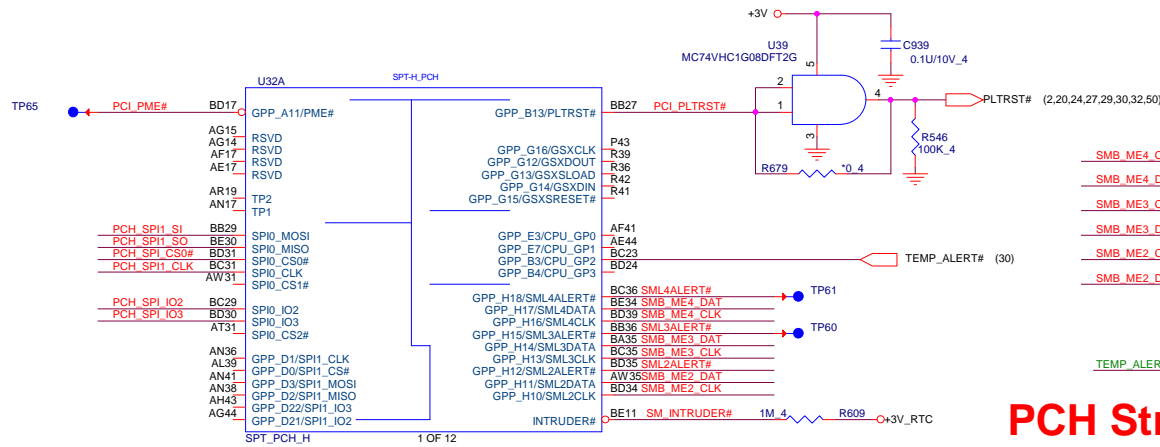






### RTC Clock 32.768KHz

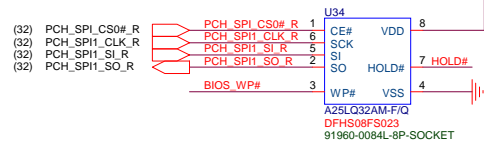




## PCH SPI ROM(CLG)

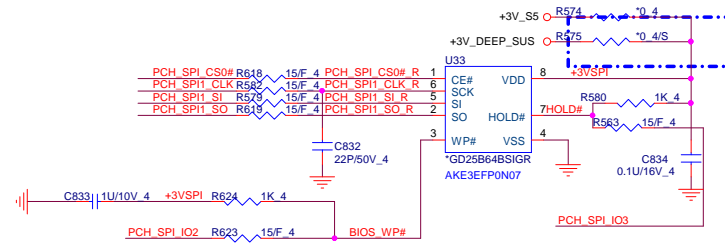
Vender	Size	P/N
EON	8MB	
Winbond	16MB	AKE3DZN0N01
GigaDevice	8MB	
Socket		DFHS08FS023

## 4M SPI ROM Socket



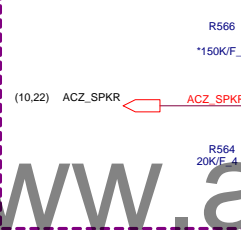
U2003&amp;U2004 footprint must overlap

## PCH SPI ROM(CLG)



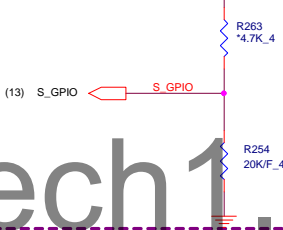
## TOP SWAP OVERRIDE STRAP

HIGH: TOP SWAP ENABLED (CRB)  
LOW: TOP SWAP DISABLED (DEFAULT)



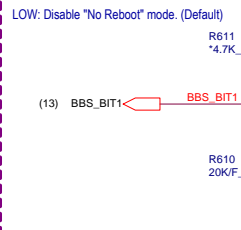
## BOOT SELECT STRAP

HIGH: LPC  
LOW: SPI (Default)



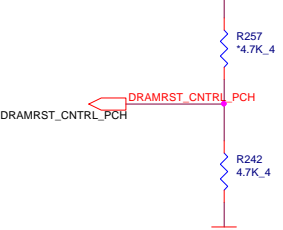
## NO REBOOT IF SAMPLED HIGH

HIGH: Enable No Reboot mode.  
This function is useful when running ITP/XDP.



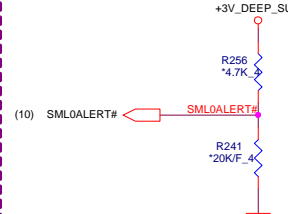
## ESPI/LPC SELECT STRAP

HIGH: eSPI is selected for EC.  
LOW: LPC is selected for EC. (Default)



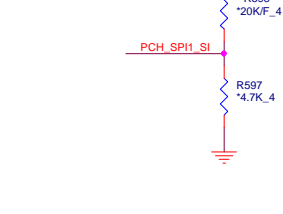
## TLS CONFIDENTIALITY ENABLED

HIGH: Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). (CRB)  
LOW: Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)



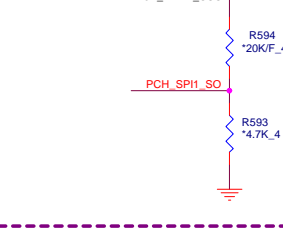
## RESERVED

This strap should sample HIGH.  
There should NOT be any on-board device driving it to opposite direction during strap sampling.



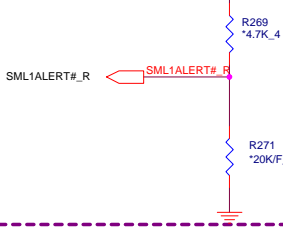
## RESERVED

This strap should sample HIGH.  
There should NOT be any on-board device driving it to opposite direction during strap sampling.



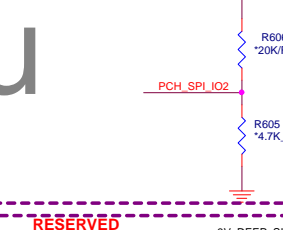
## RESERVED

This strap should sample LOW.  
There should NOT be any on-board device driving it to opposite direction during strap sampling.



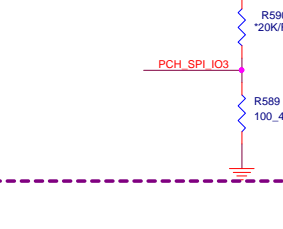
## RESERVED

This strap should sample HIGH.  
There should NOT be any on-board device driving it to opposite direction during strap sampling.



## RESERVED

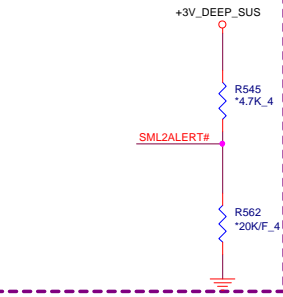
This strap should sample HIGH.  
There should NOT be any on-board device driving it to opposite direction during strap sampling.



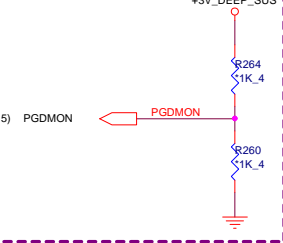
## ESPI FLASH SHARING MODE

HIGH: SLAVE ATTACHED FLASH SHARING  
LOW: 0: MASTER ATTACHED FLASH SHARING

This strap should sample LOW.  
driving it to opposite direction during strap sampling.  
There should NOT be any on-board device

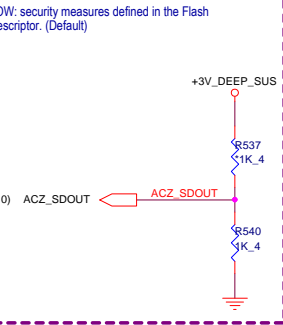


DFX TEST MODE QUALIFIER FOR OTHER DFX STRAP WHEN SAMPLED LOW



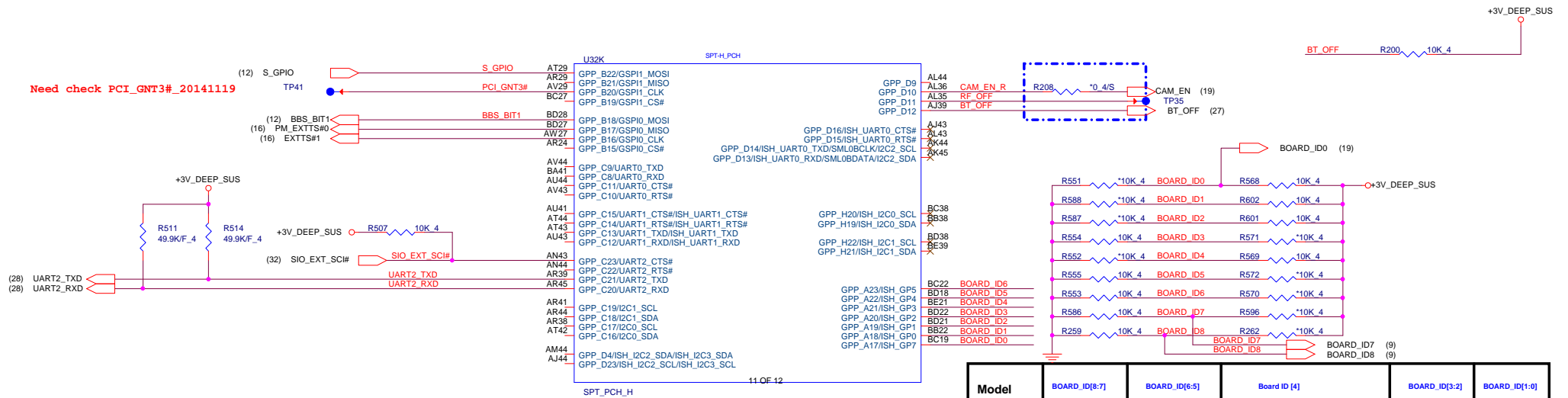
## TLS CONFIDENTIALITY ENABLED

HIGH: Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. (CRB)  
LOW: security measures defined in the Flash Descriptor. (Default)

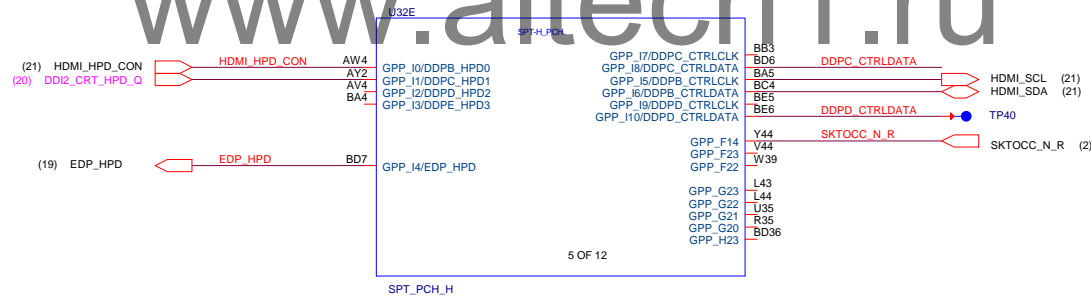
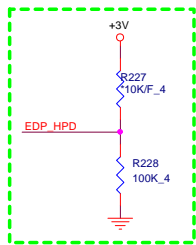


**PROJECT : NL9**  
**Quanta Computer Inc.**

Size	Document Number	PCH 4/6 (GPIO/MISC)	Rev
Date:	Wednesday, October 14, 2015	12	61
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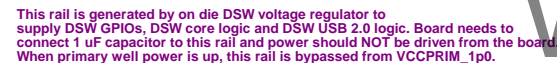


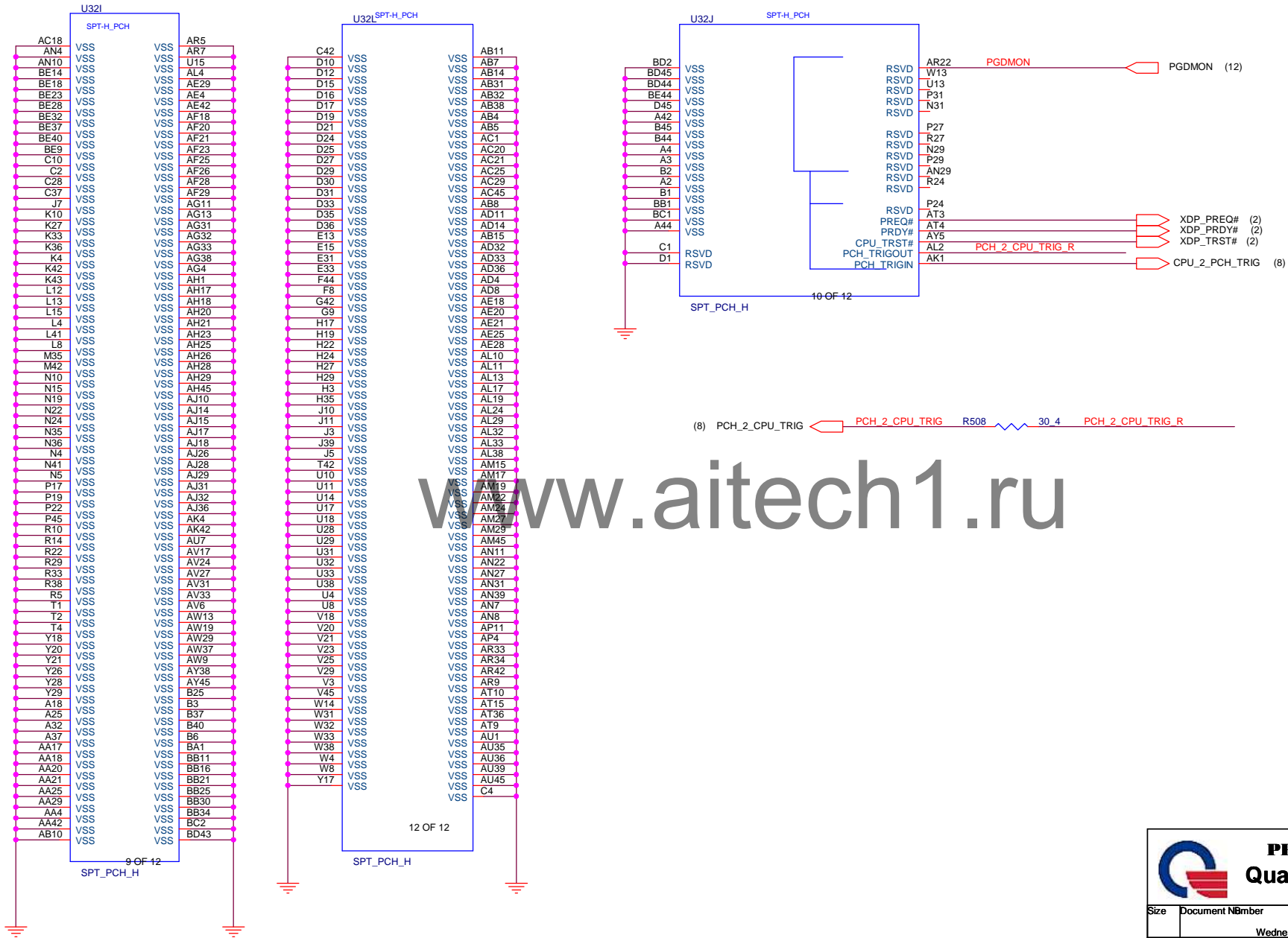
Reserve EDP\_HPD opposites circuit!

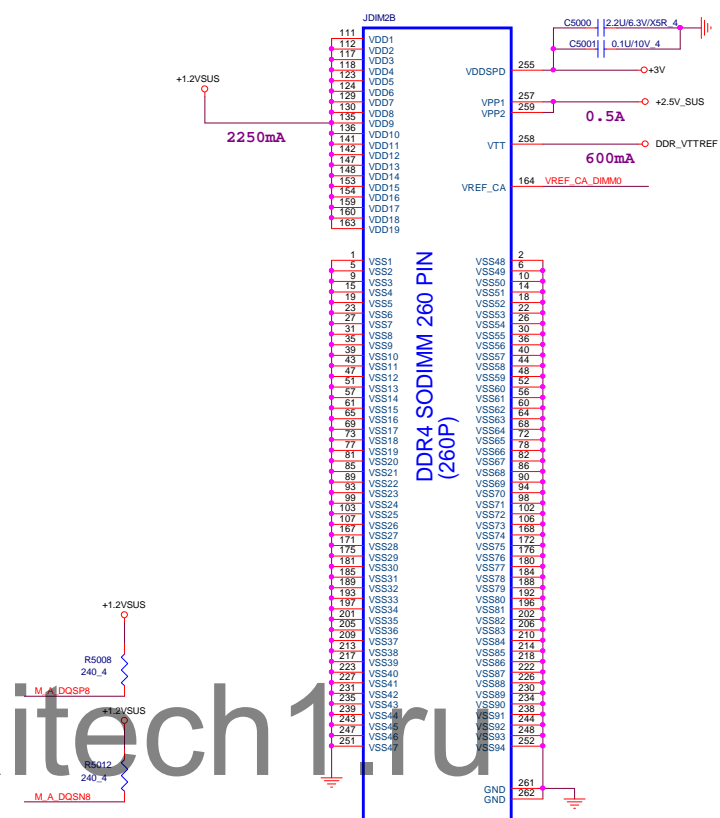
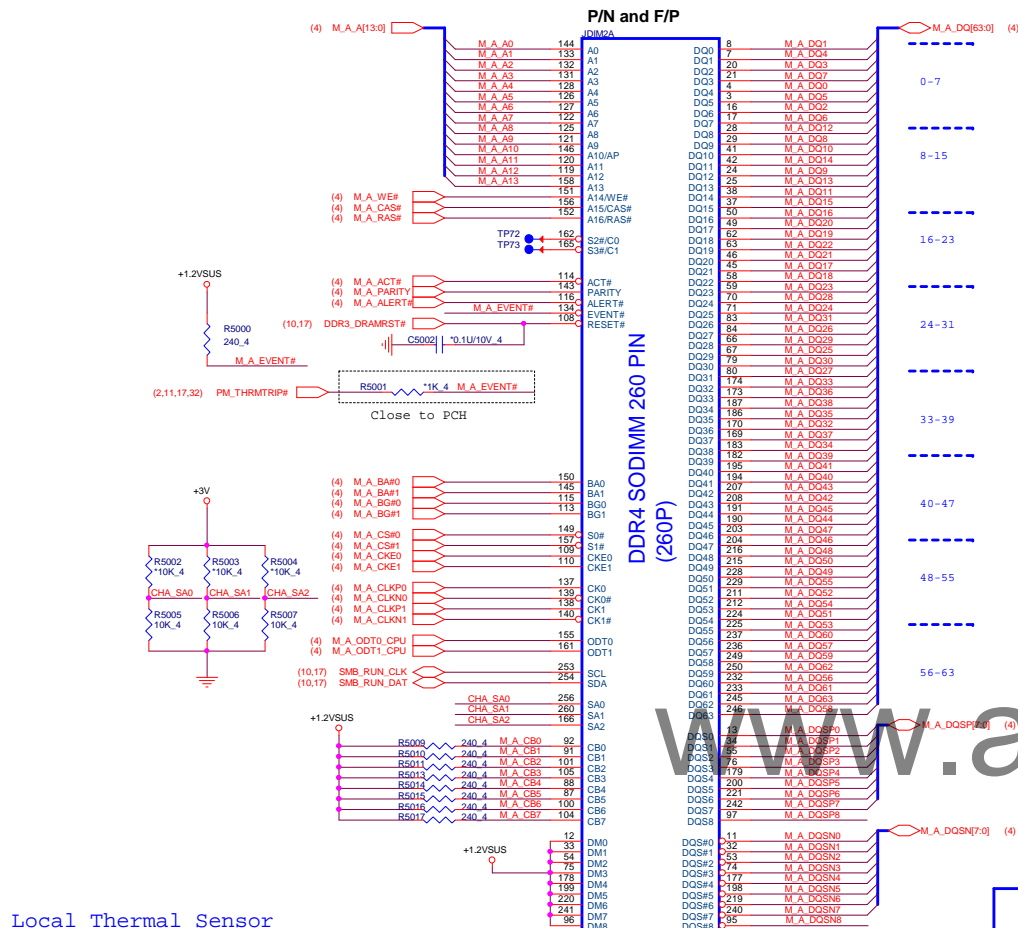


This signal has a weak internal pull-down.  
0 = Port C and D is not detected.  
1 = Port C and D is detected.

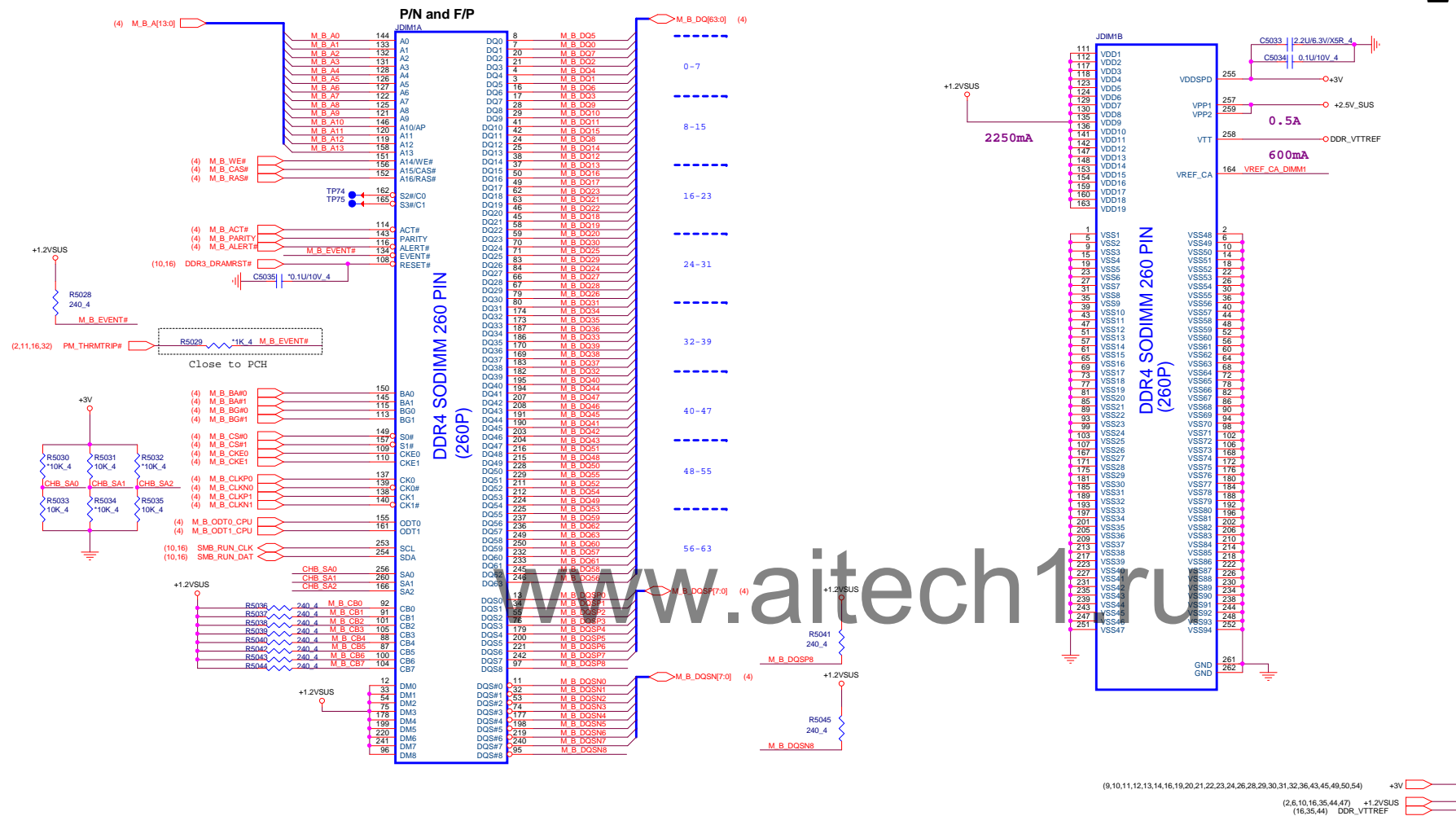


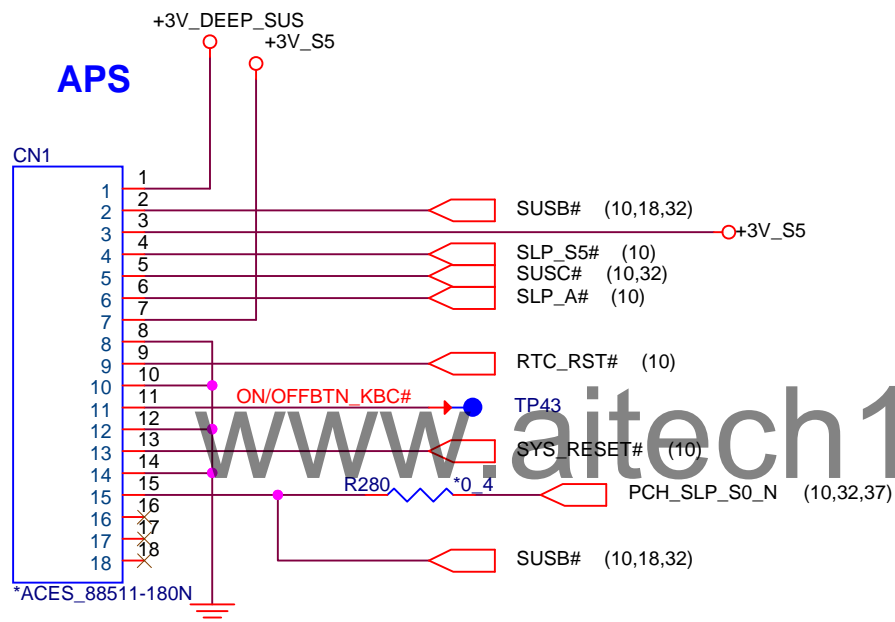










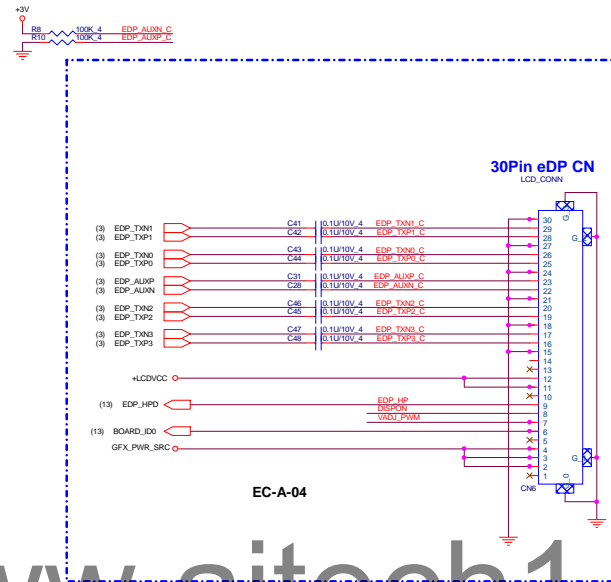
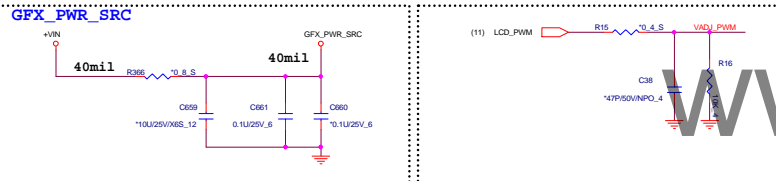
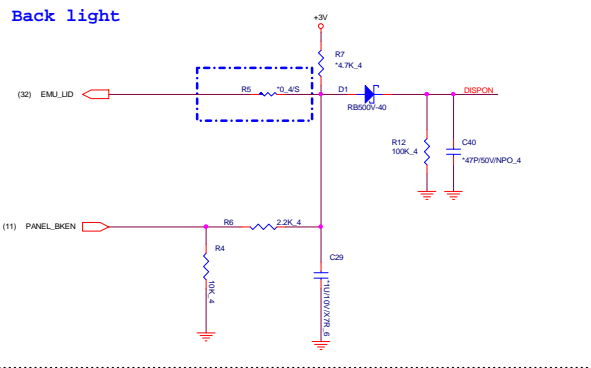
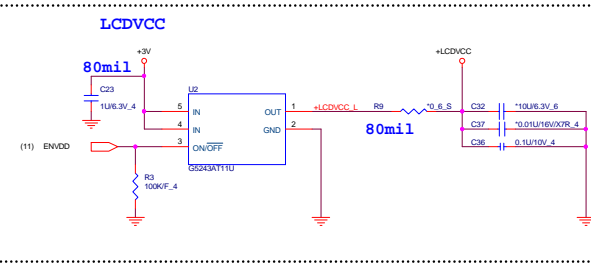


(9,10,12,13,14,16,43) +3V\_DEEP\_SUS



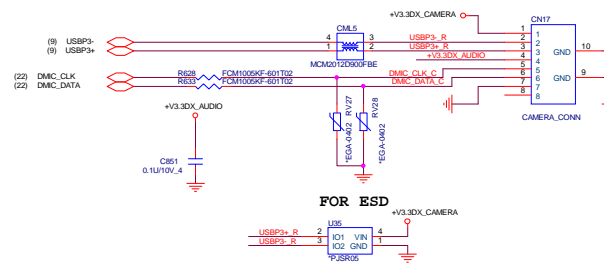
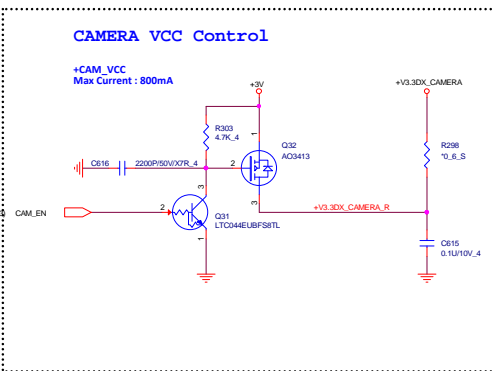
**PROJECT : NL9**  
**Quanta Computer Inc.**

Size	Document Number	22 -- HSW XDP & APS	Rev	1A
Date:	Wednesday, October 14, 2015	18	61	
	Sheet	of		

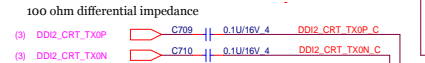
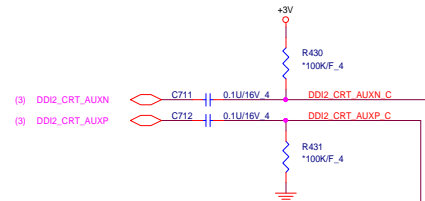
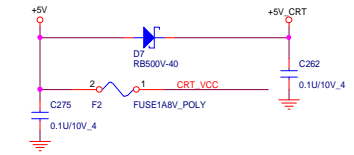
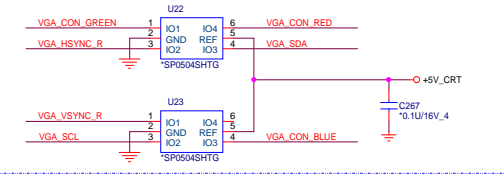


EC-A-04

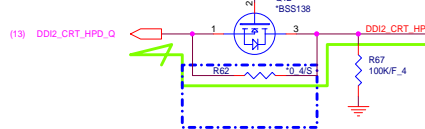
## CAMERA/DMIC CONN



## ESD PROTECTION



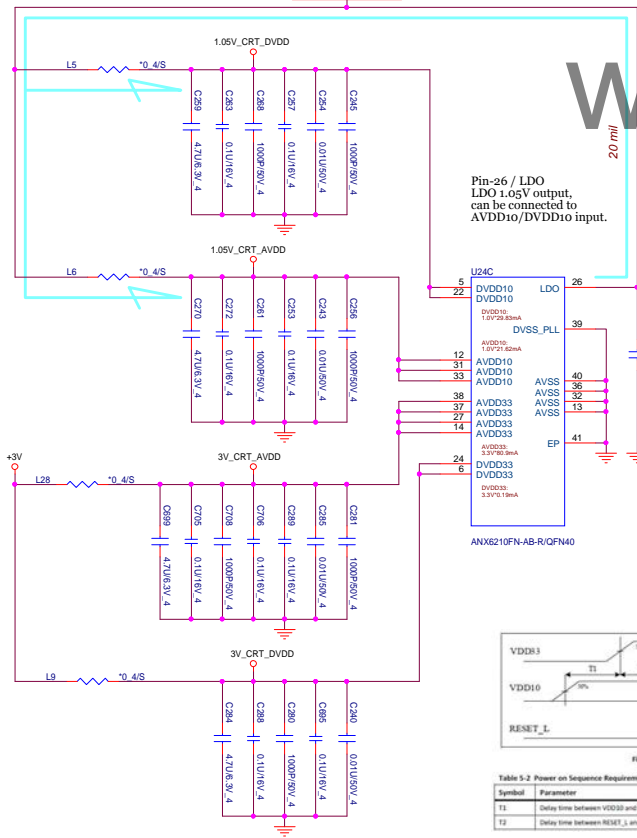
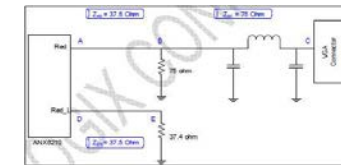
Confirm to delete Q9.

Place R<sub>c</sub>, R<sub>d</sub>, R<sub>e</sub> as close as possible to relative pins of ANX6210.Place R<sub>x</sub>, R<sub>y</sub>, R<sub>z</sub> as close as possible to the R/G/B pins of VGA header.

Layout Note : Refer chip spec page-20 ~ 23.

It is strongly recommended to shield RGB with ground.

Route the VGA\_RED, VGA\_BLUE, VGA\_GREEN, VGA\_CON\_RED, VGA\_CON\_BLUE, VGA\_CON\_GREEN by 75 Ohm impedance.

Pin-26 / LDO  
LDO 1.05V output,  
can be connected to  
AVDD10/DVDD10 input.

ANX6210F0N-AB-R/OFN40

Case 1: Keep R<sub>a</sub> and remove R<sub>b</sub>;  
ANX6210 in HPD process mode;  
Case 2: Keep R<sub>b</sub> and remove R<sub>a</sub>;  
Use IRQ to inform source of VGA  
plug/unplug events

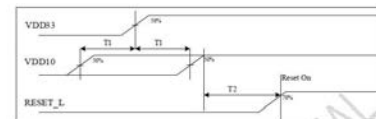


Figure 5-1: Power on Sequence

Table 5-2: Power on Sequence Requirements

Symbol	Parameter	Min	Typ	Max	Units
T1	Delay time between VDD10 and VDD16	1	1	—	ms
T2	Delay time between RESET_L and all power rails stable	1	2	—	ms

(2,12,24,27,29,30,32,50)

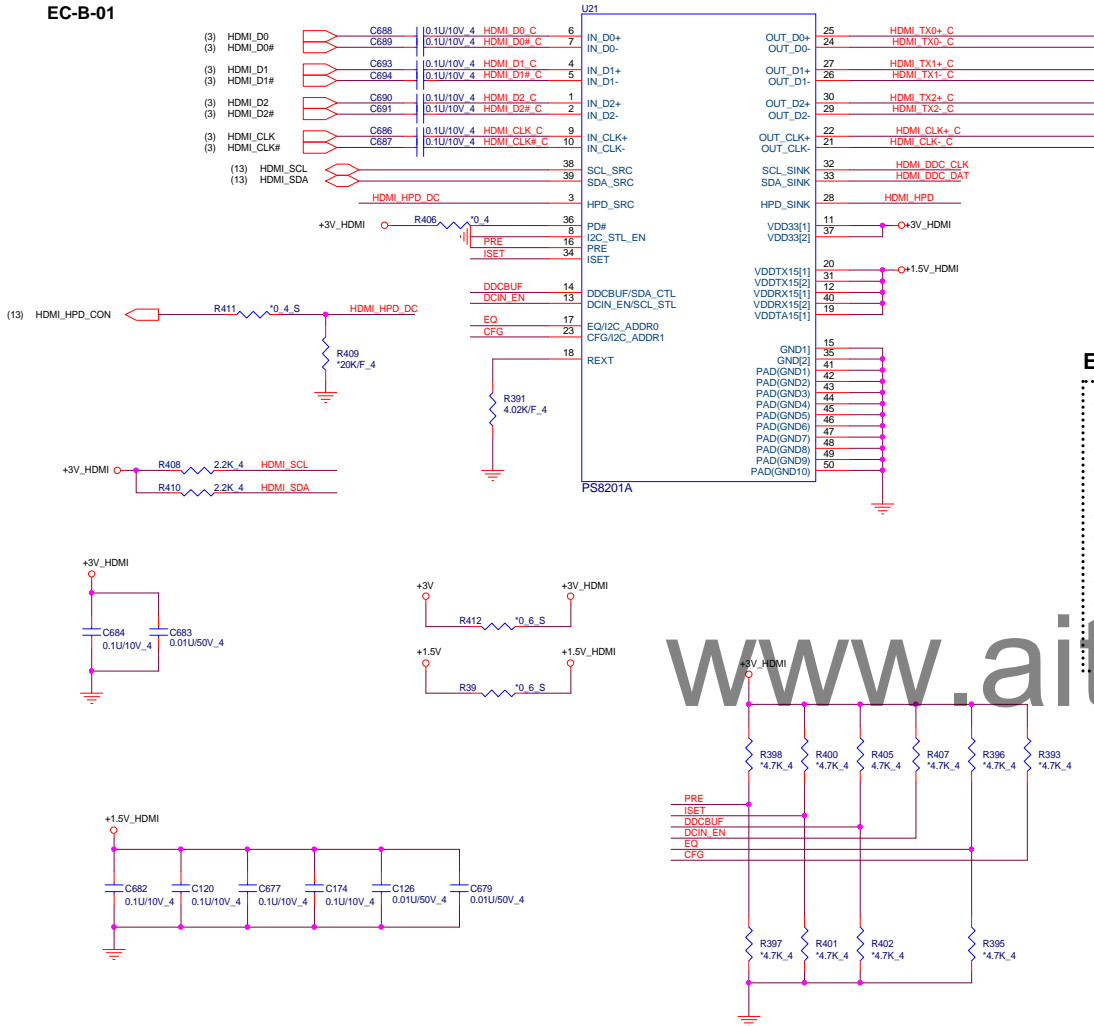
(9,10,11,12,13,14,16,17,19,21,22,23,24,26,28,29,30,31,32,36,43,45,49,50,54)  
(21,22,23,25,30,31,43,45,49,58)

+3V

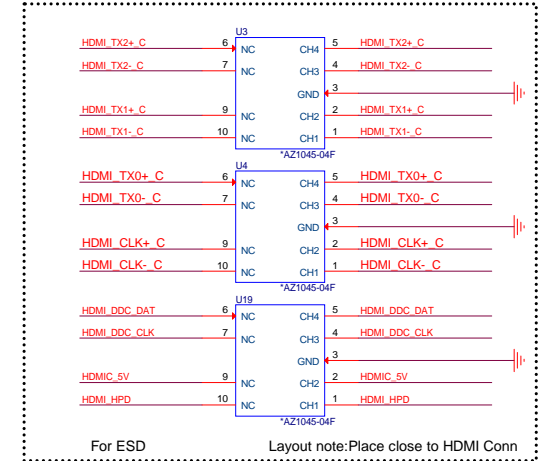
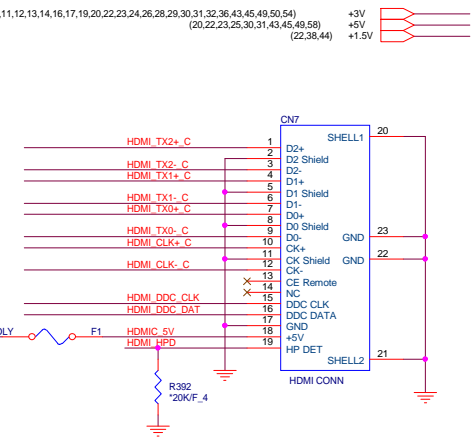
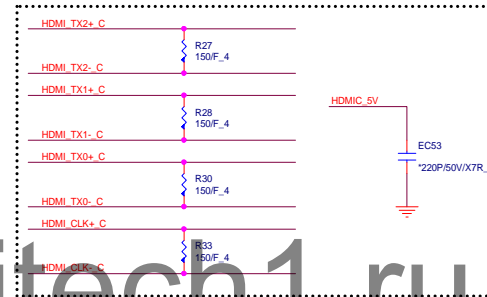
+5V

Pin-11 / GPIO  
1: I2C Address is 0x50 and 0x8C  
0: 4.7KΩ resistor to pull down, I2C address is 0x52 and 0x8E

# EC-B-01



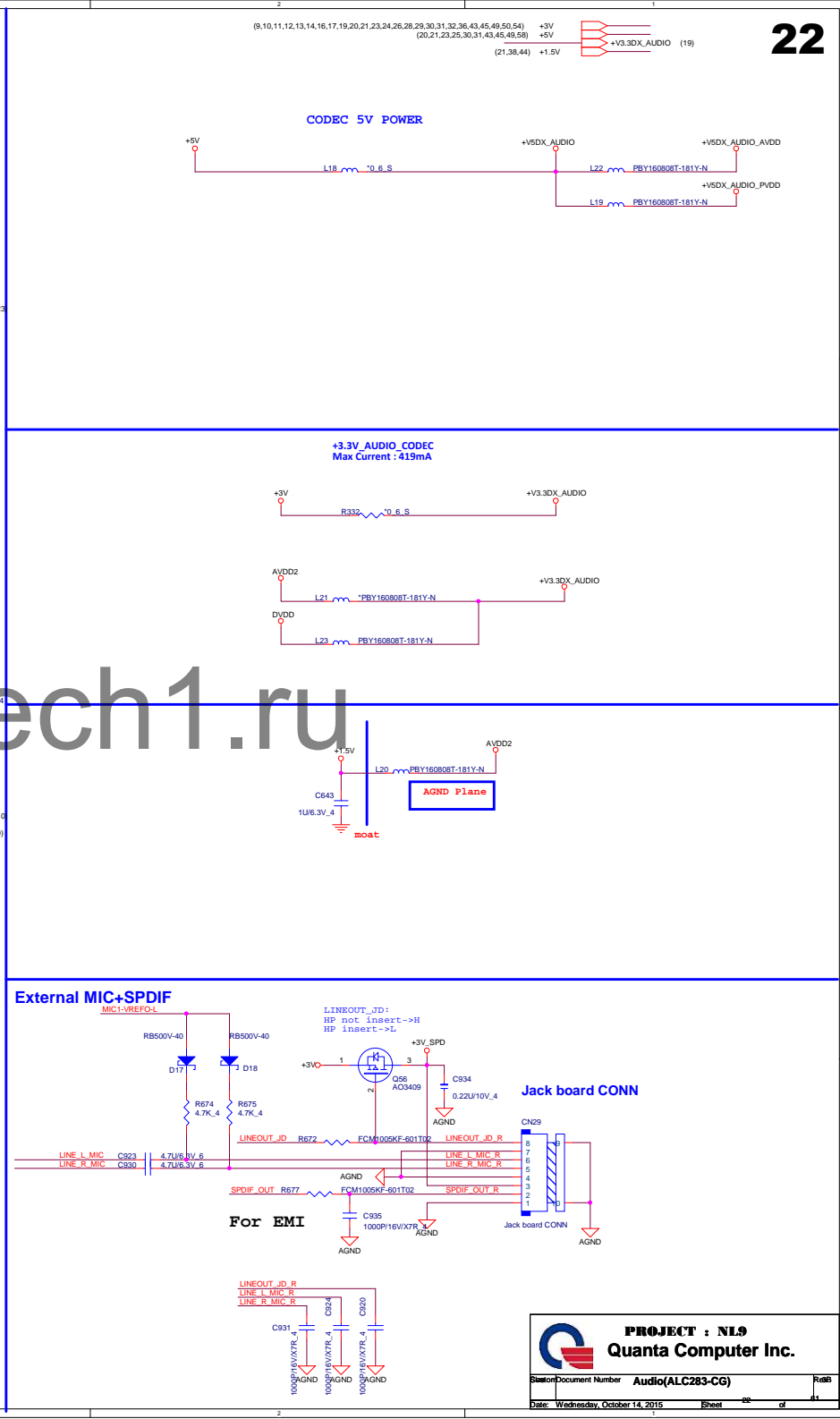
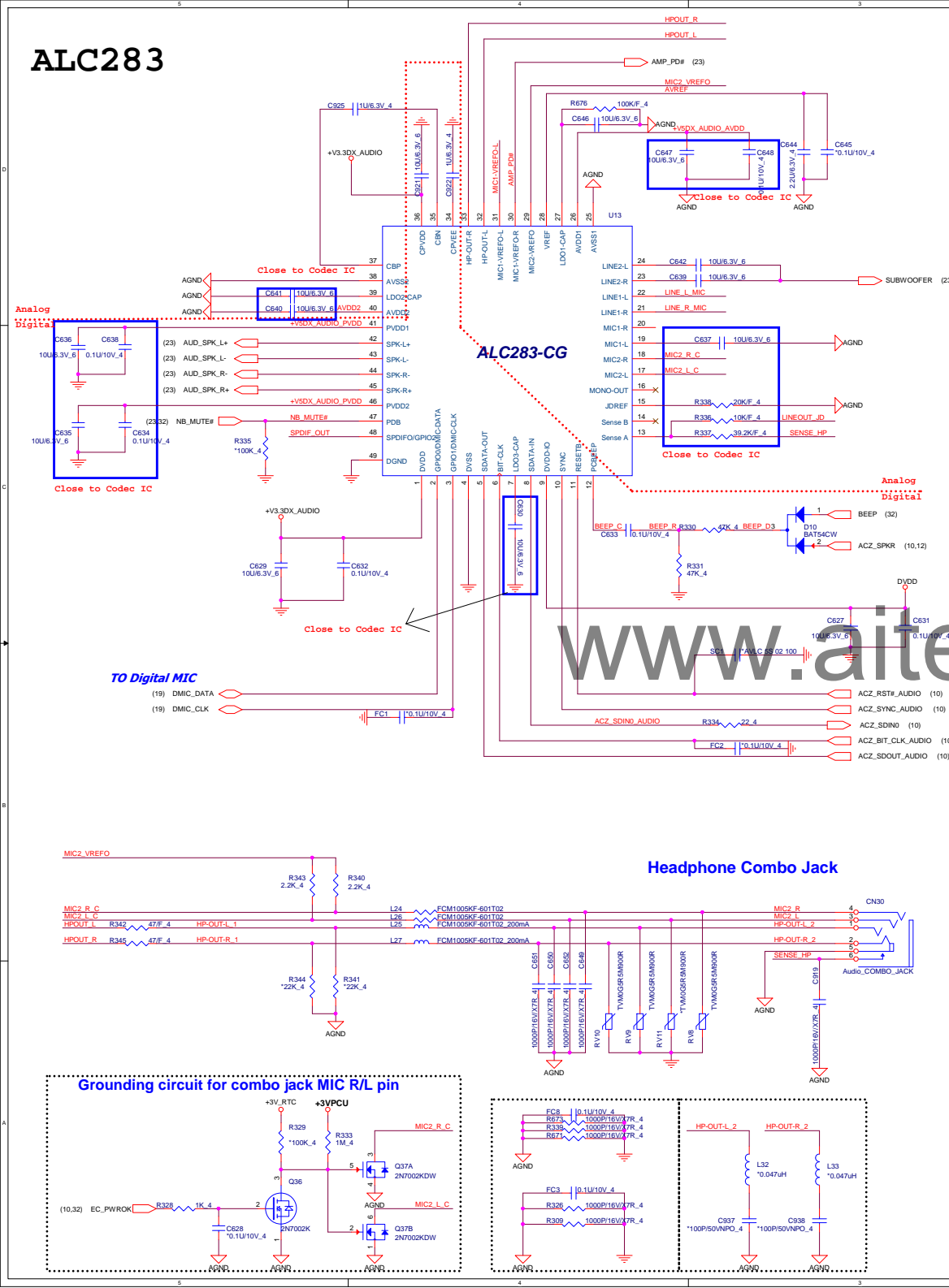
## EMI reserve for HDMI



For ESD

Layout note: Place close to HDMI Conn

**ALC283**





Reserve for Input attenuation  
To have optimization output power

Placement C4609  
and then C4611

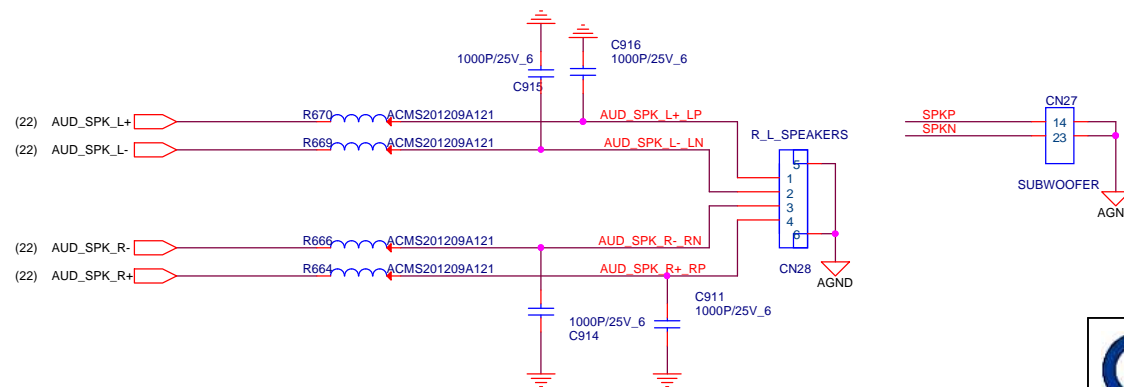
Close to IC

need to Close to connector  
Reserve for EMI Depression

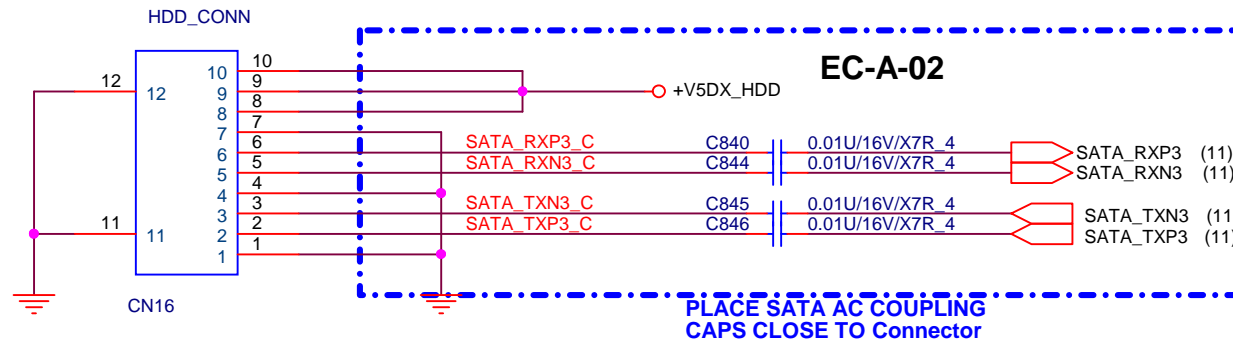
need to very  
Close to IC

Output Gain Table

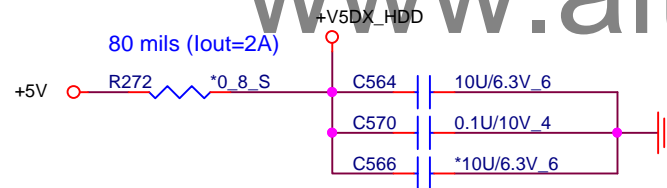
R364	R363	R373	R372	Gain(Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB





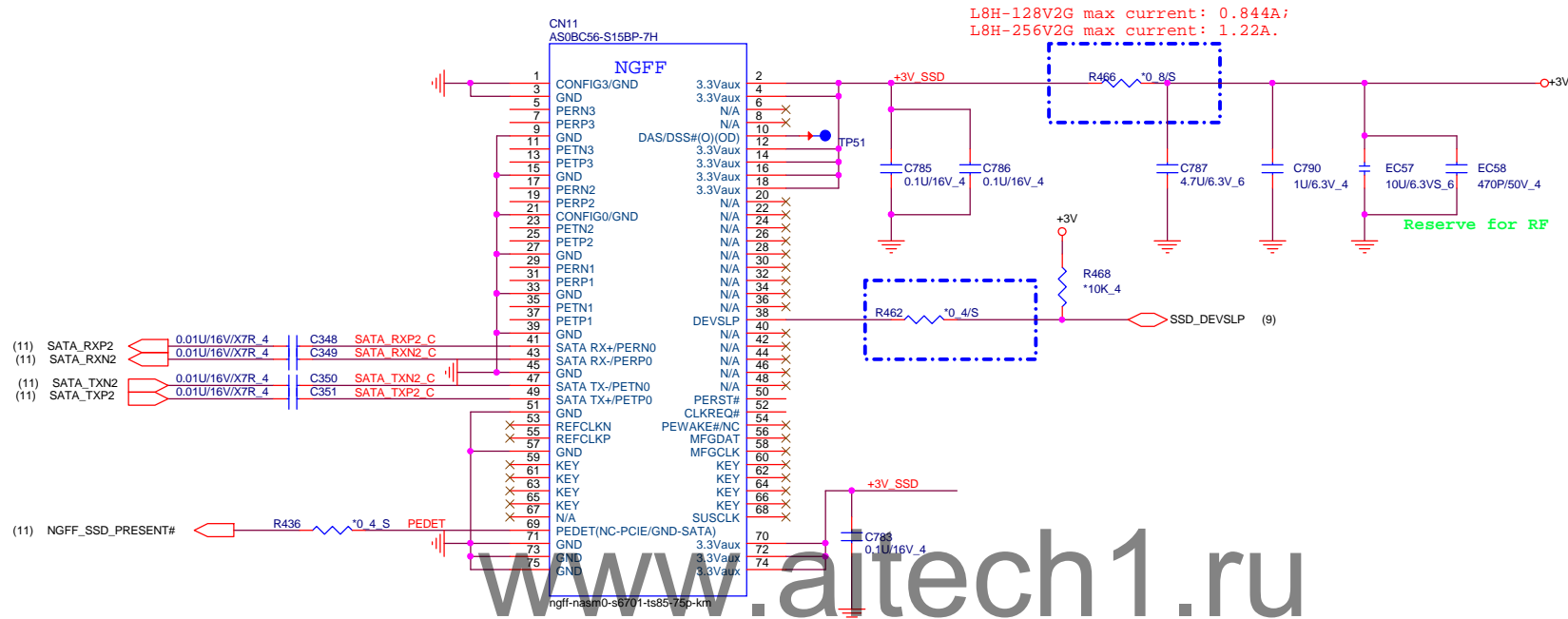


DC Current rating: 2 A (MAX)



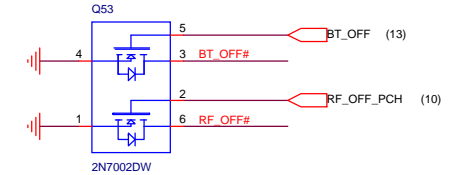
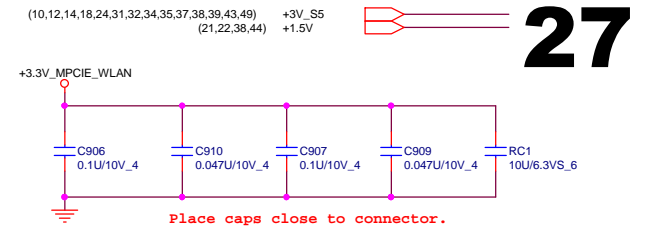
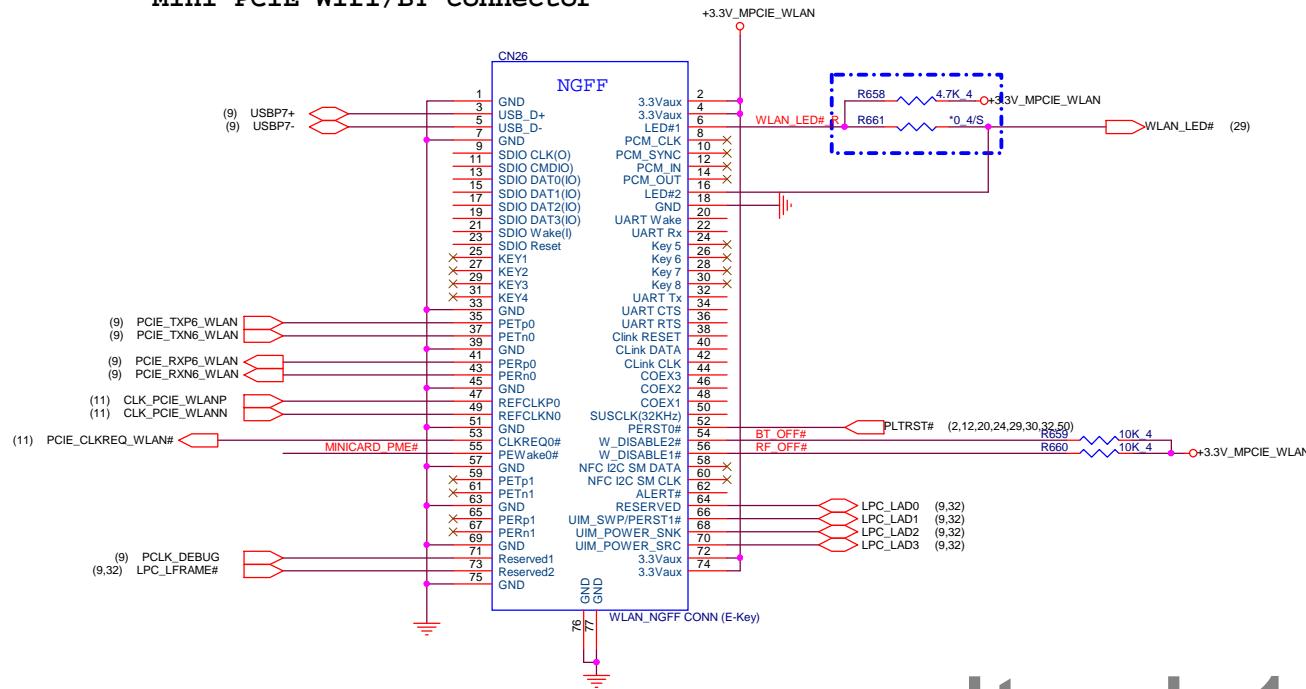
**PROJECT : NL9**  
**Quanta Computer Inc.**

Size	Document Number	SATA HDD	Rev
Date:	Wednesday, October 14, 2015	Sheet	25 of 61

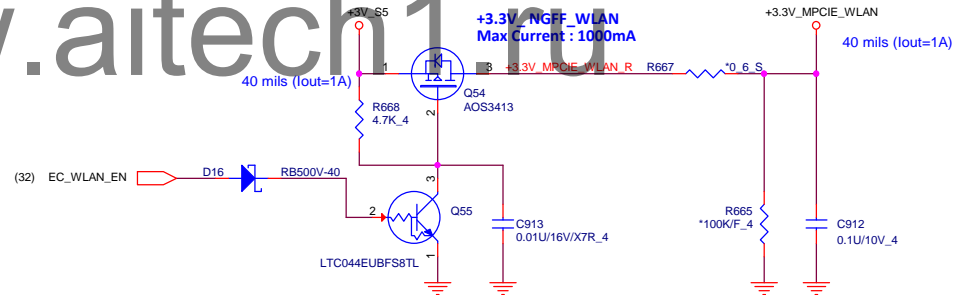
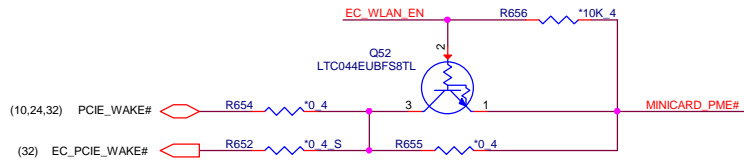


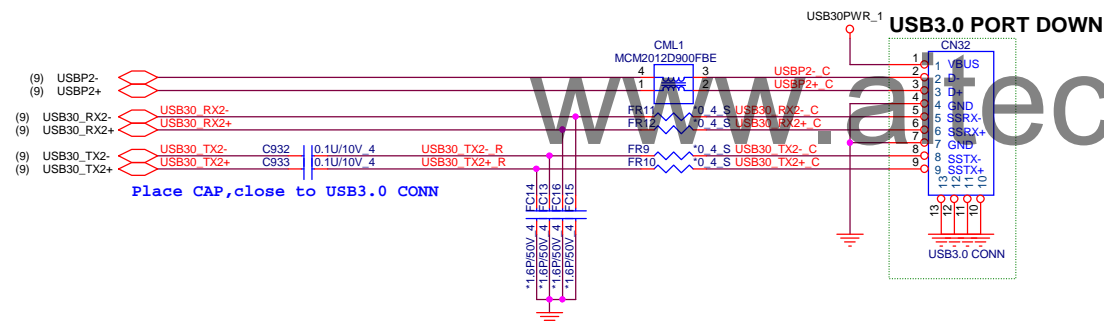
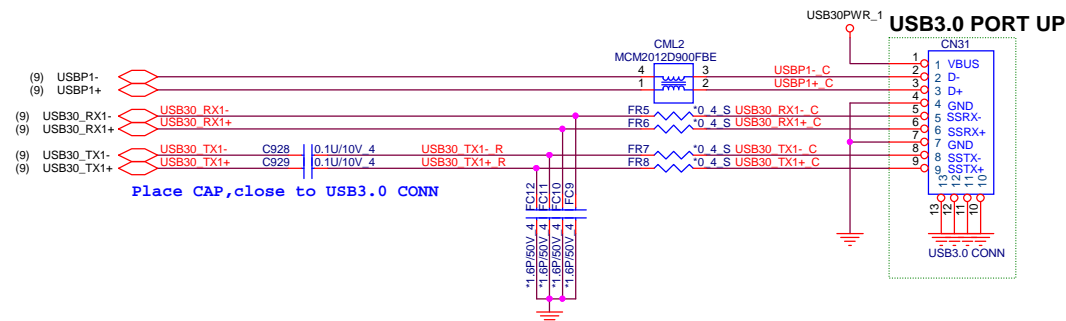
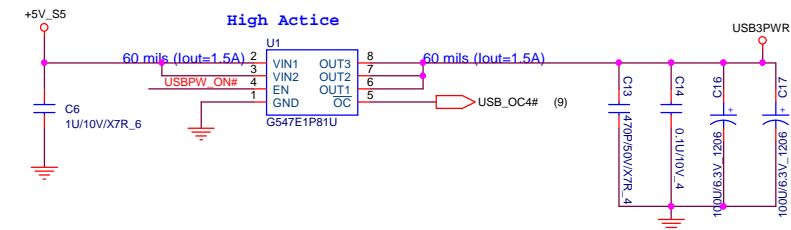
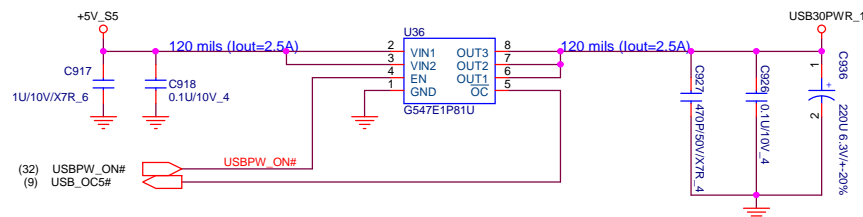
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# Mini PCIE Wifi/BT connector

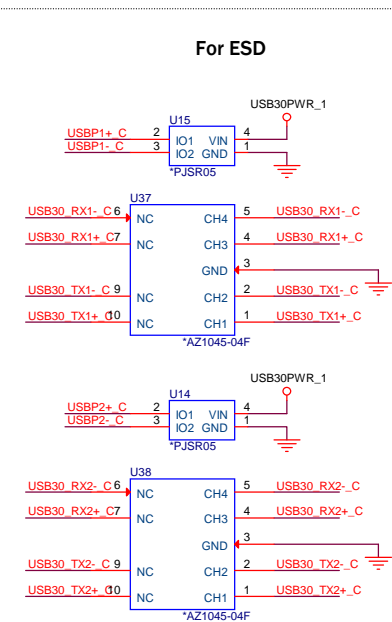
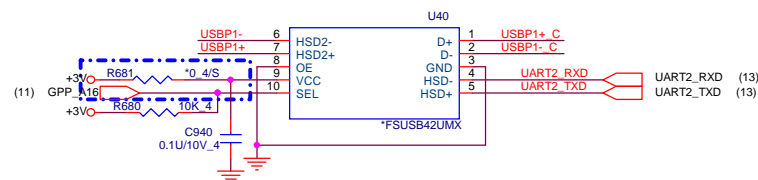


www.aitech1.ru



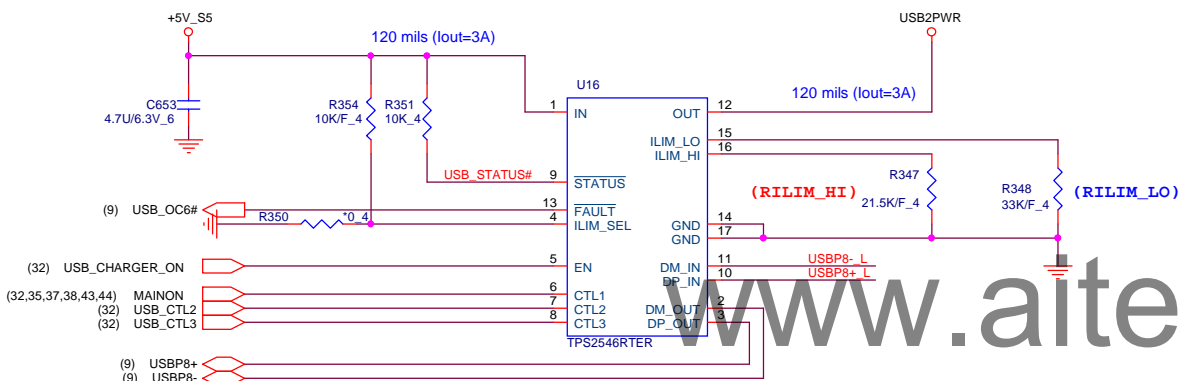


## UART for DEBUG





## USB Charger 2.0 Port



RILIM\_LO is optional and the ILIM\_LO pin may be left unconnected if the following conditions are met:

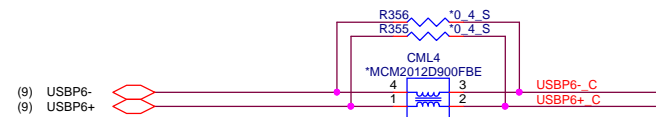
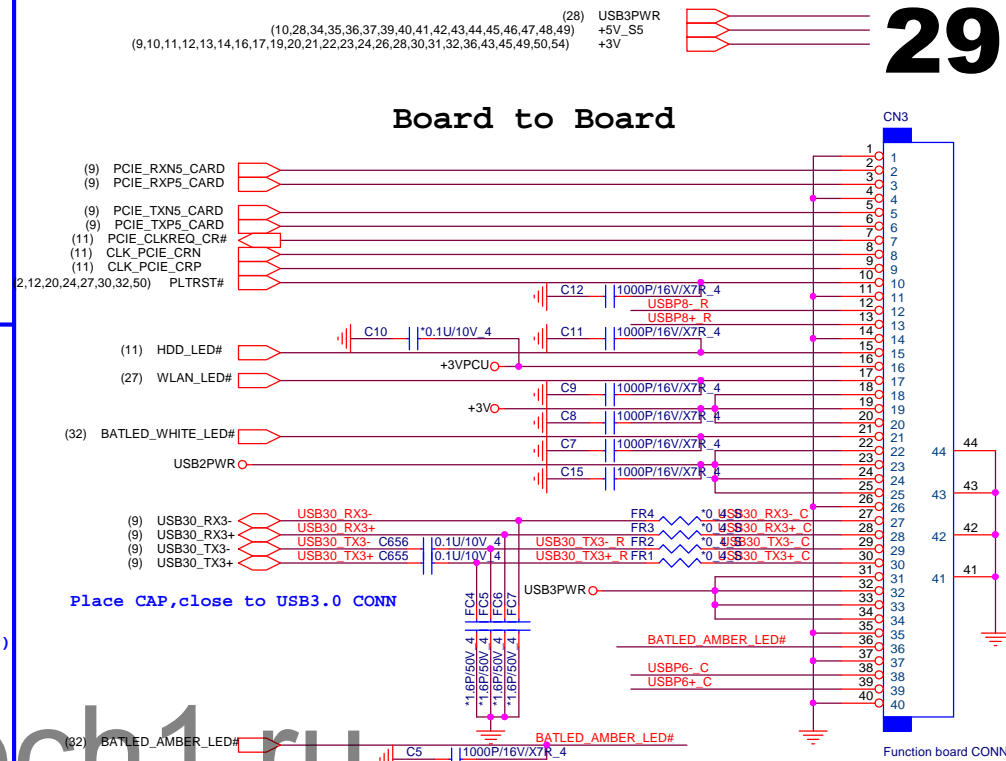
1. ILIM\_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used

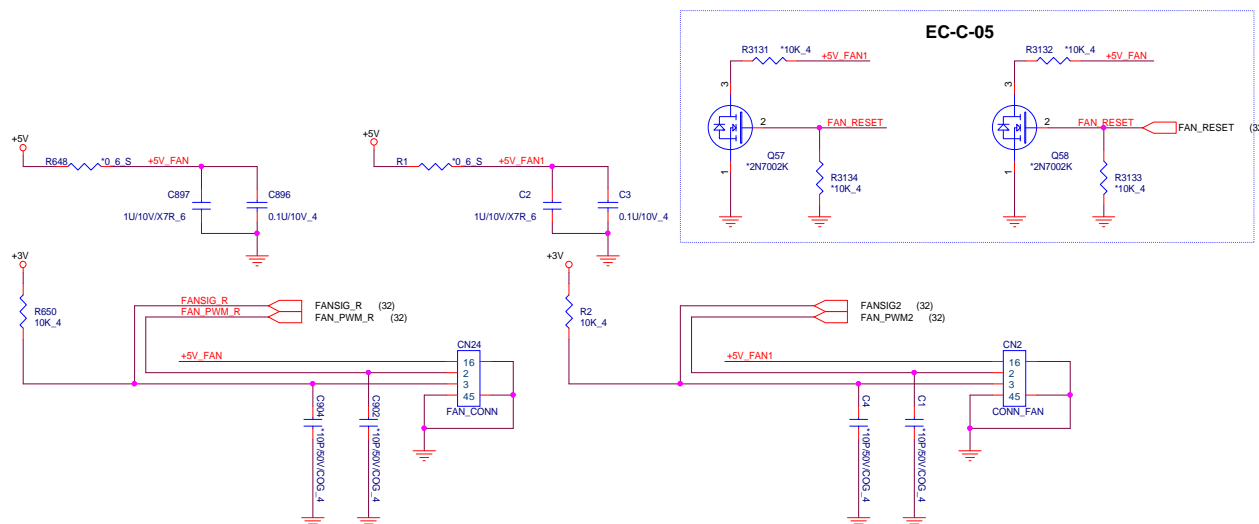
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM\_LO < 20.6 kΩ.

The following equation programs the typical current limit:

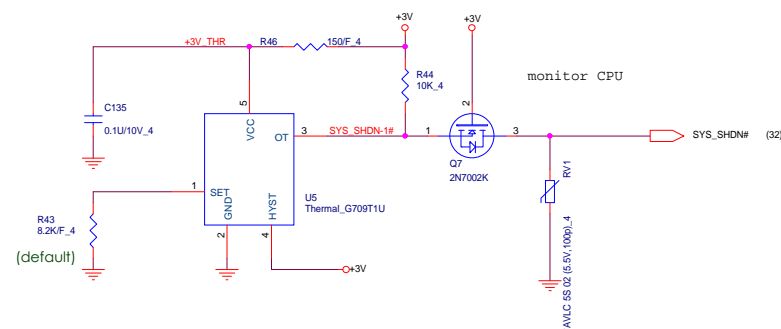
$$I_{LIM\_XX} \text{ (mA)} = \frac{50,500}{RILIM\_XX}$$

$$I_{OS\_typ}(mA) = \frac{50,500}{(R_{ILIM\_XX}(k\Omega) + 0.1)}$$



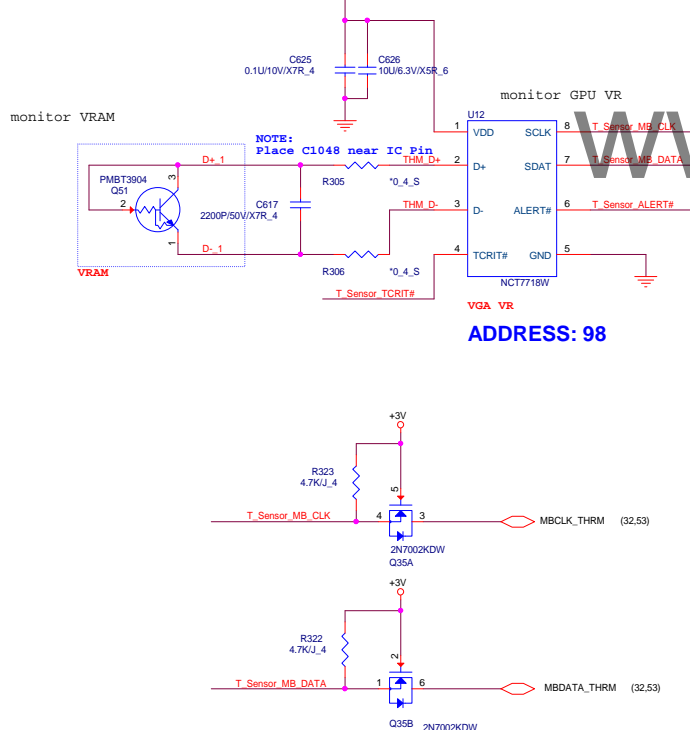


# Thermal Sensor



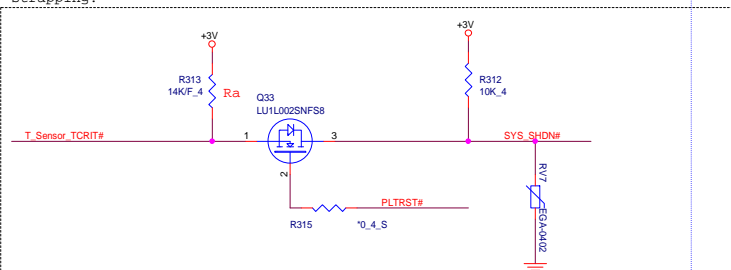
# Thermal Sensor

## EC-A-06



\*Reserved the circuit to isolate the ALERT#/T\_CRIT# pin for power-on T\_CRIT temperature strapping.

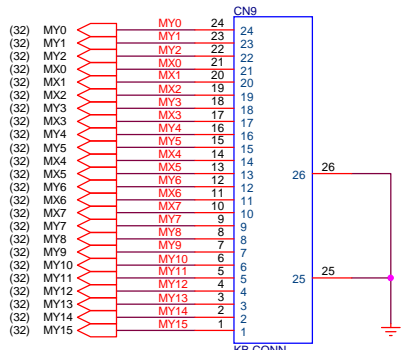
it is to avoid abnormal operation when power on within 100ms for HW strap pin setting HW Shut-down Temp. 109 °C



## ALERT# /T\_CRIT# Pull-up Resistor

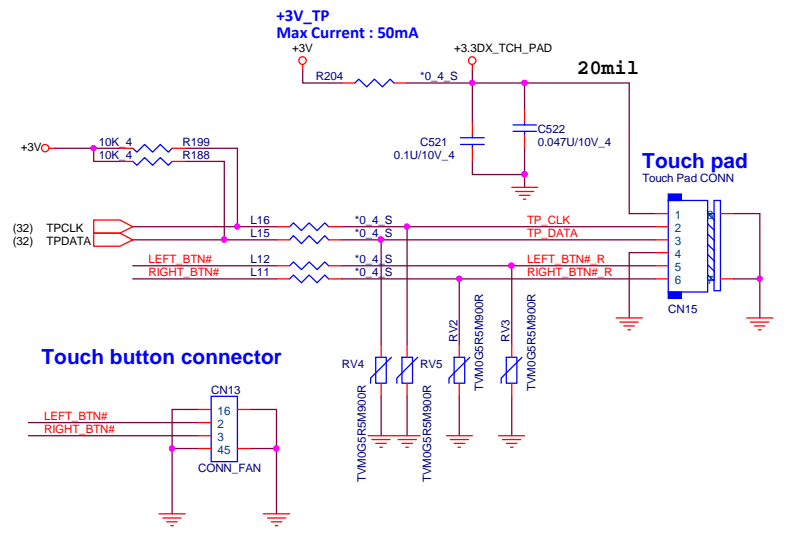
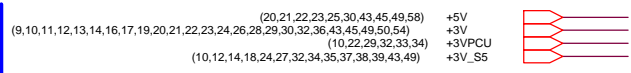
Rb	2Kohm	7.5Kohm	10Kohm	14Kohm	18.7Kohm
T_CRIT temperature strapping point	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

KEYBOARD

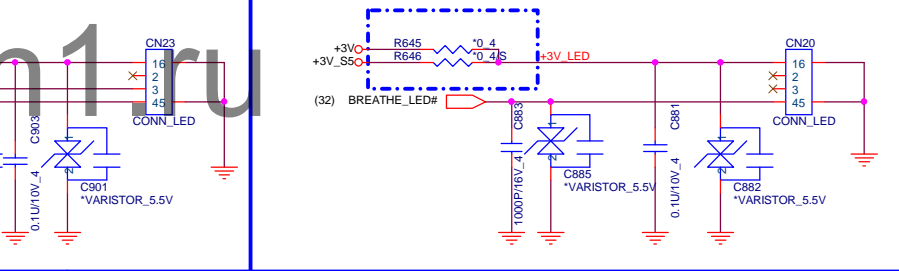
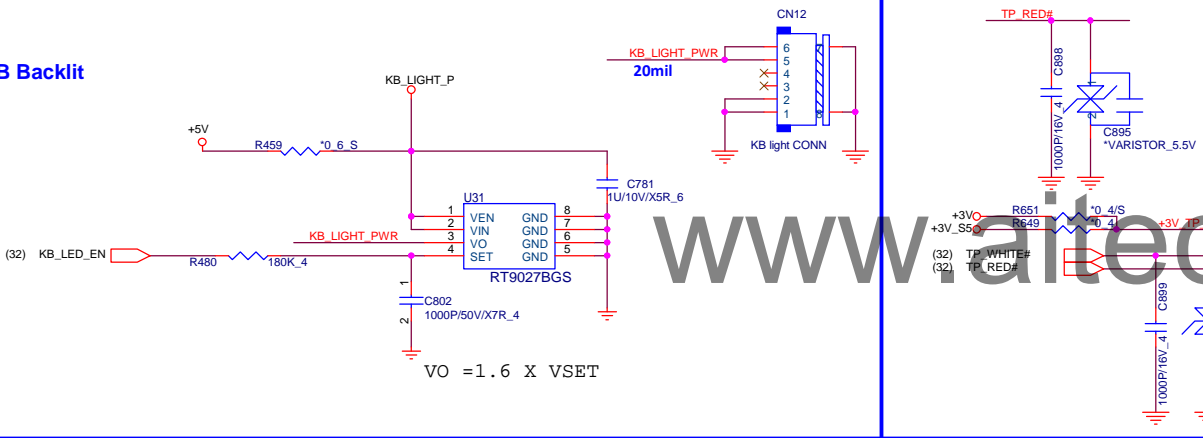


For EMI

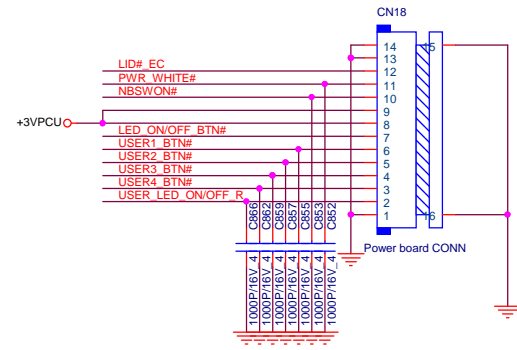
MY15 C322	220P/50V/X7R_4	C317	220P/50V/X7R_4	MY13
MY10 C304	220P/50V/X7R_4	C316	220P/50V/X7R_4	MY12
MY2 C315	220P/50V/X7R_4	C264	220P/50V/X7R_4	MY3
MY14 C319	220P/50V/X7R_4	C287	220P/50V/X7R_4	MY6
MX0 C255	220P/50V/X7R_4	C258	220P/50V/X7R_4	MX1
MY1 C242	220P/50V/X7R_4	C293	220P/50V/X7R_4	MX7
MY5 C276	220P/50V/X7R_4	C291	220P/50V/X7R_4	MX6
MX3 C269	220P/50V/X7R_4	C302	220P/50V/X7R_4	MY9
MX2 C260	220P/50V/X7R_4	C297	220P/50V/X7R_4	MY8
MY0 C238	220P/50V/X7R_4	C294	220P/50V/X7R_4	MY7
MX5 C286	220P/50V/X7R_4	C273	220P/50V/X7R_4	MY4
MX4 C282	220P/50V/X7R_4	C244	220P/50V/X7R_4	MY2



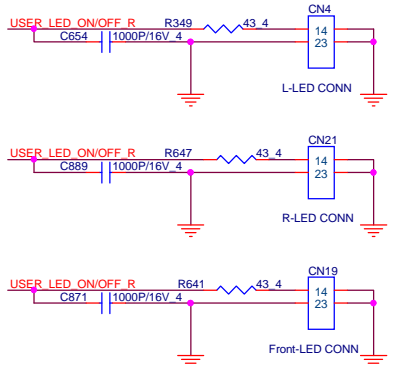
KB Backlit



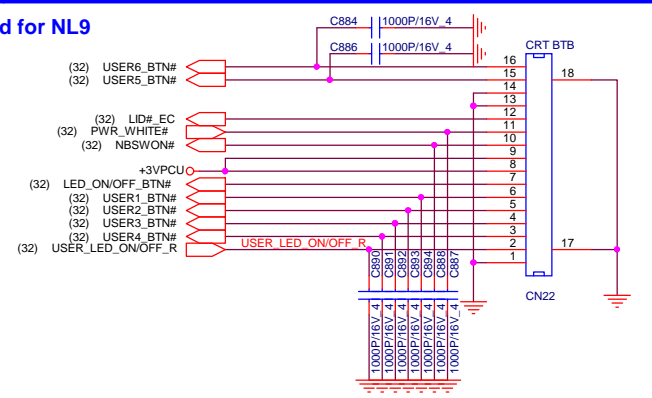
Power board for NL8

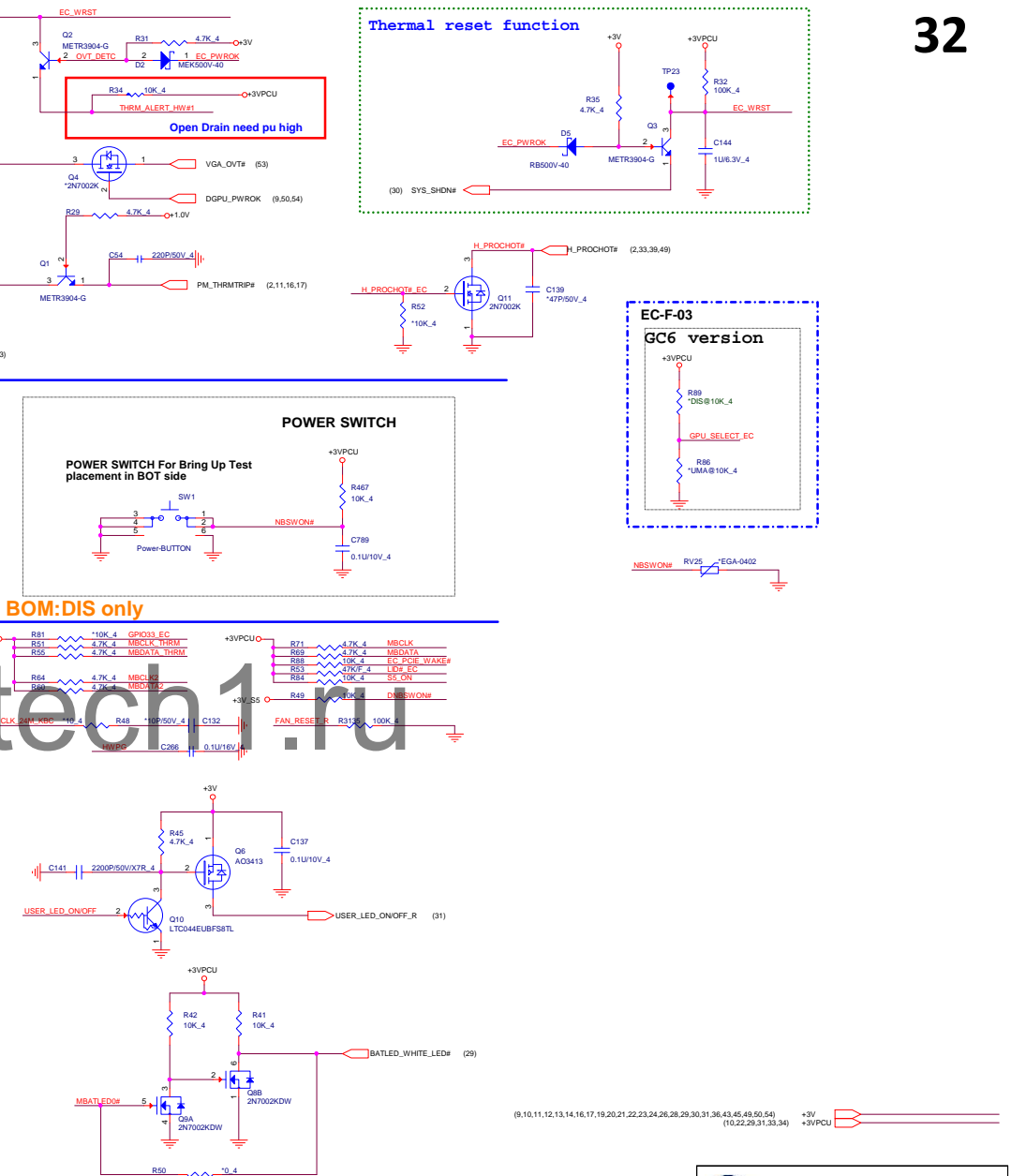
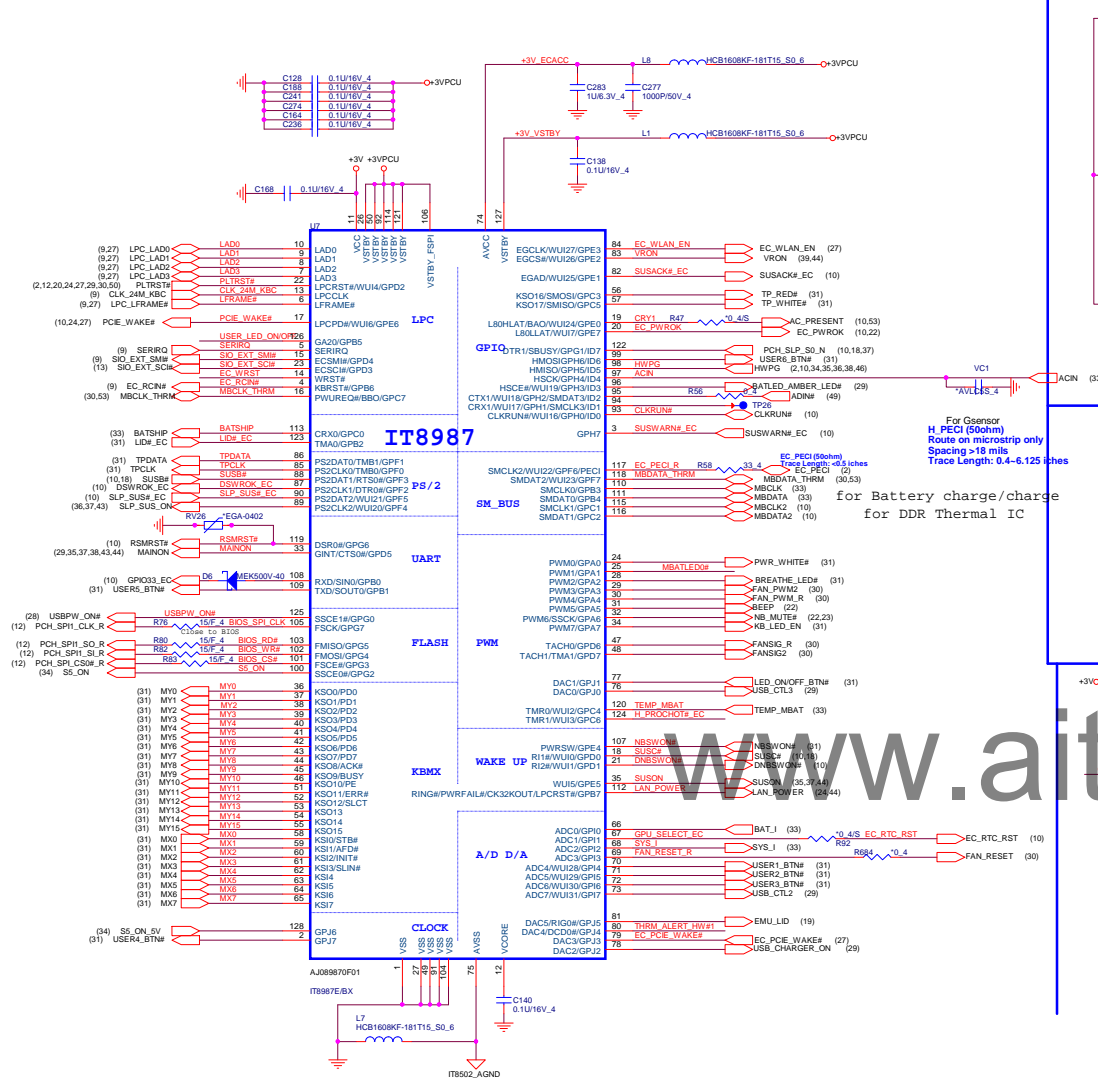


LED CONN



Power board for NL9





(49,58) +VA  
(19,34,35,36,39,40,41,42,46,47,49,58) +VIN  
(10,22,28,31,32,34) +3VPCU

180W for N16E-GT  
150W for N16P-GX  
120W for N16P-GT

Do Not add test pad on BATDIS\_G signal

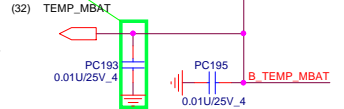
EMI request for ISN

120W&150W follow 180W setting

Place this ZVS close to Diode away +VIN

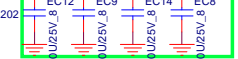
Place this ZVS close to Far-Far away +VIN

Place this cap close to EC



For ISN

Place this cap close to EC



ACDET=17.2V


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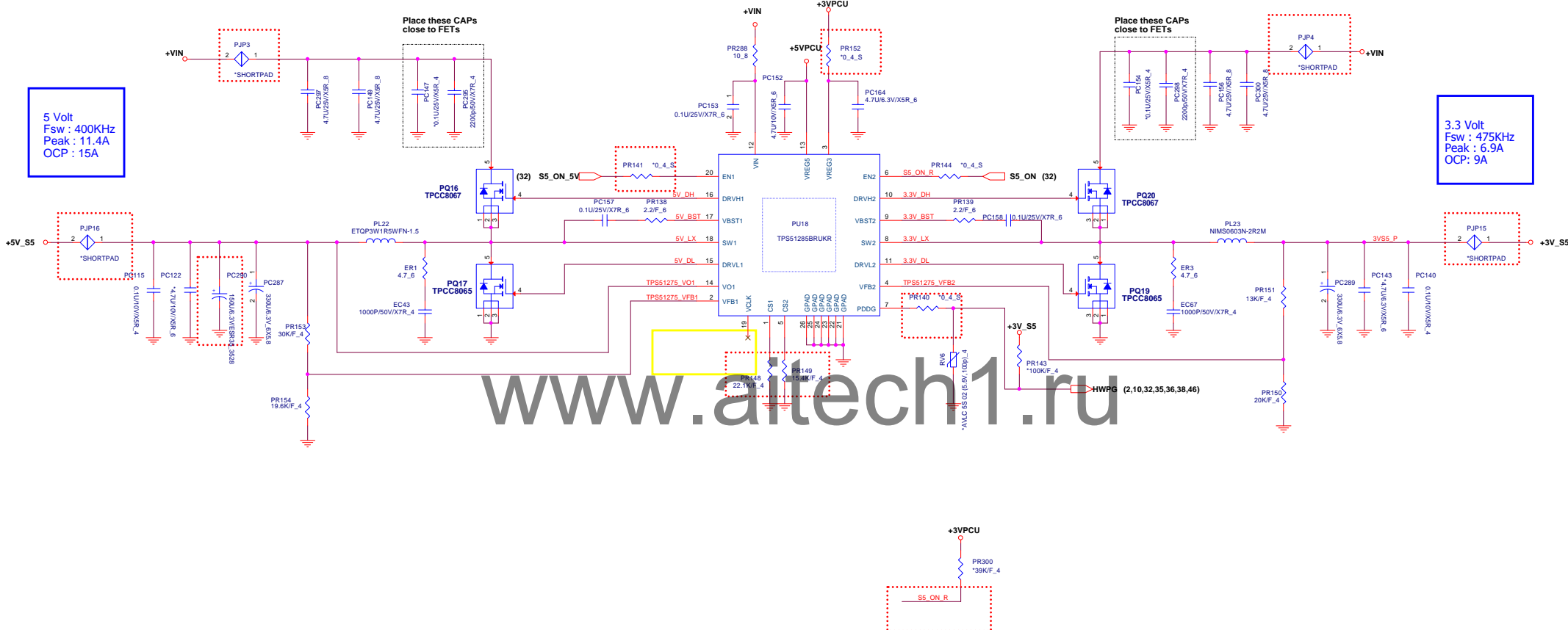
VIDCHG = 8 or 16 x (VSRN - VSRP)

Place this cap close to EC

Place this cap close to EC

16.5K 180W for N16E-GT  
20K 150W for N16P-GX  
25K 120W for N16P-GT

 <b>PROJECT : NL8A</b> <b>Quanta Computer Inc.</b>			
Size Custom	Document Number	Charger (BQ24780S)	
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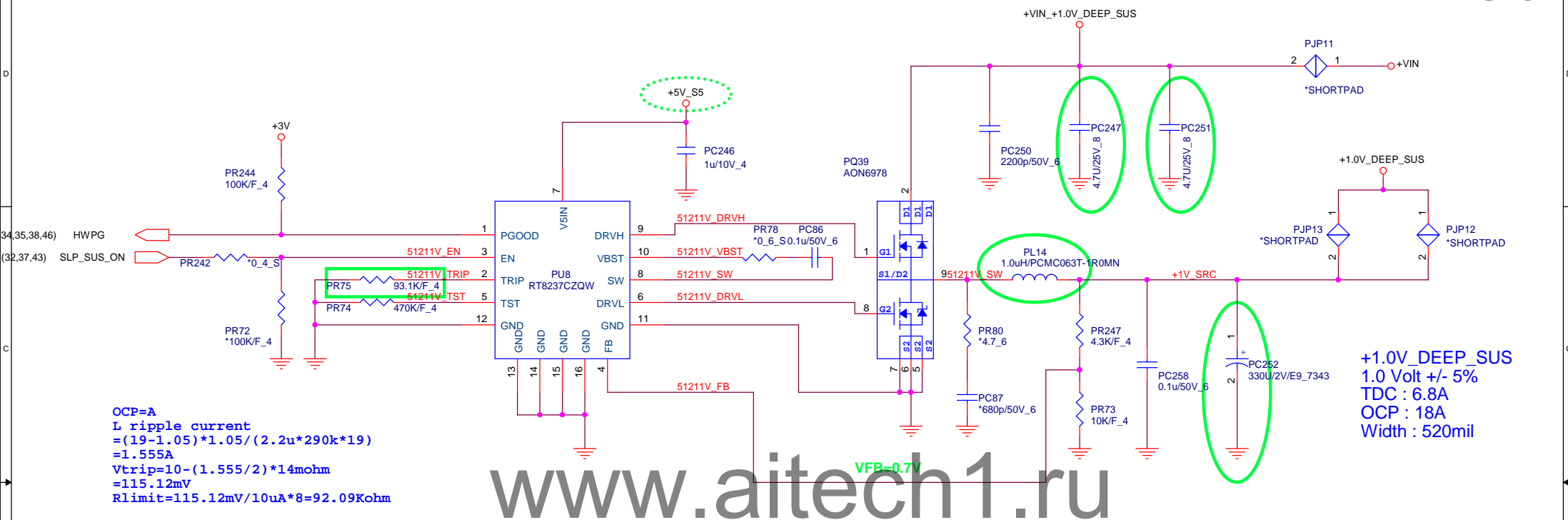


$$V_o = (0.675 * (1 + (R1/R2)))$$

+2.5V\_SUS  
2.5Volt +/- 5%  
TDC : 0.75A  
PEAK : 1A  
Width : 40mil

$$V_o = (0.6(R_1 + R_2)/R_2)$$

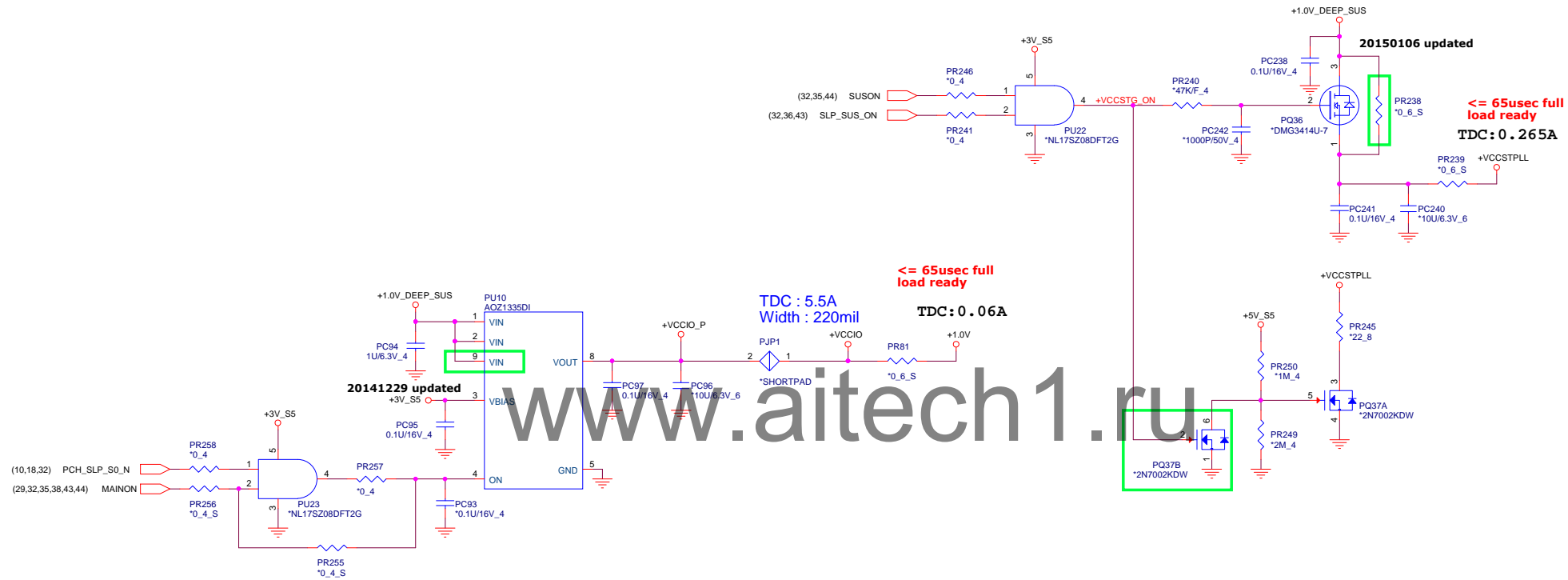


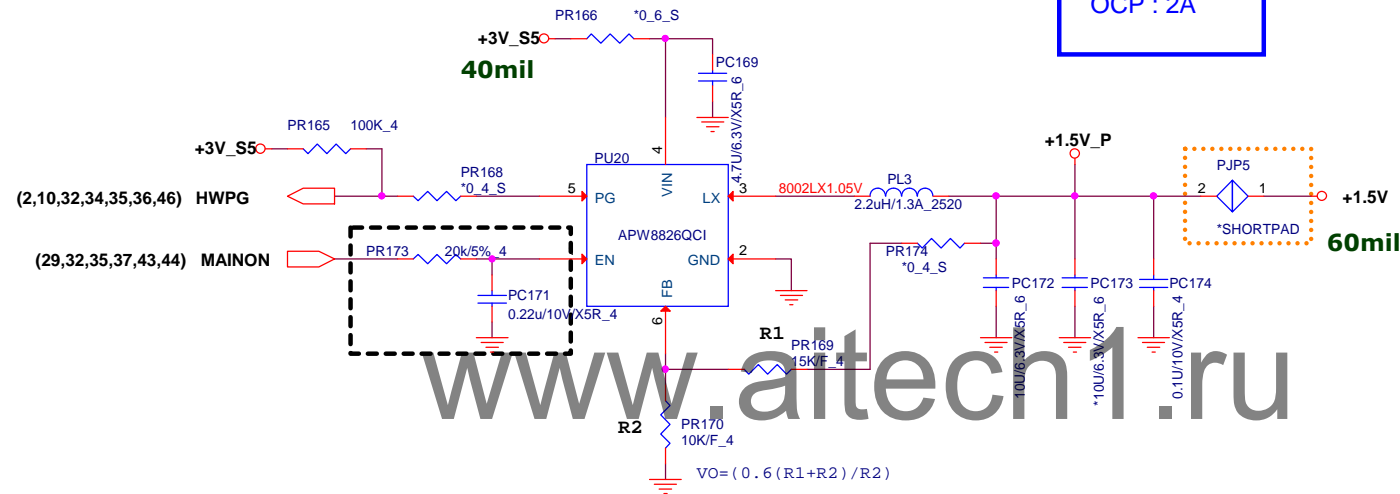


**Quanta Computer Inc.**

**PROJECT : ZRW**

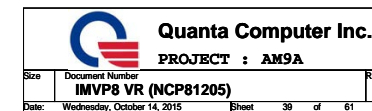
Size	Document Number	Rev
	<b>+1V_S5 (RT8237CZQW)</b>	1A
Date:	Wednesday, October 14, 2015	Sheet 36 of 61

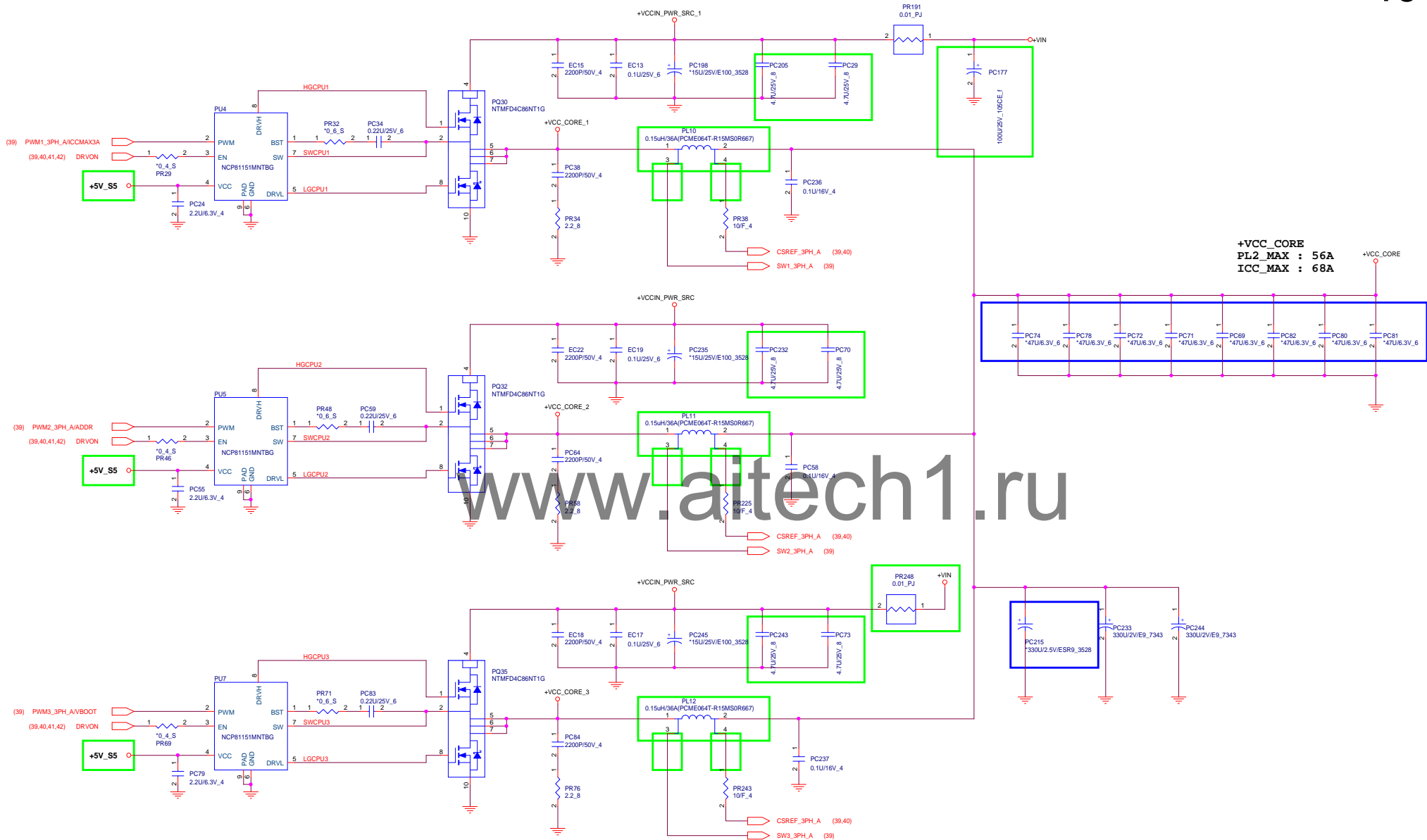


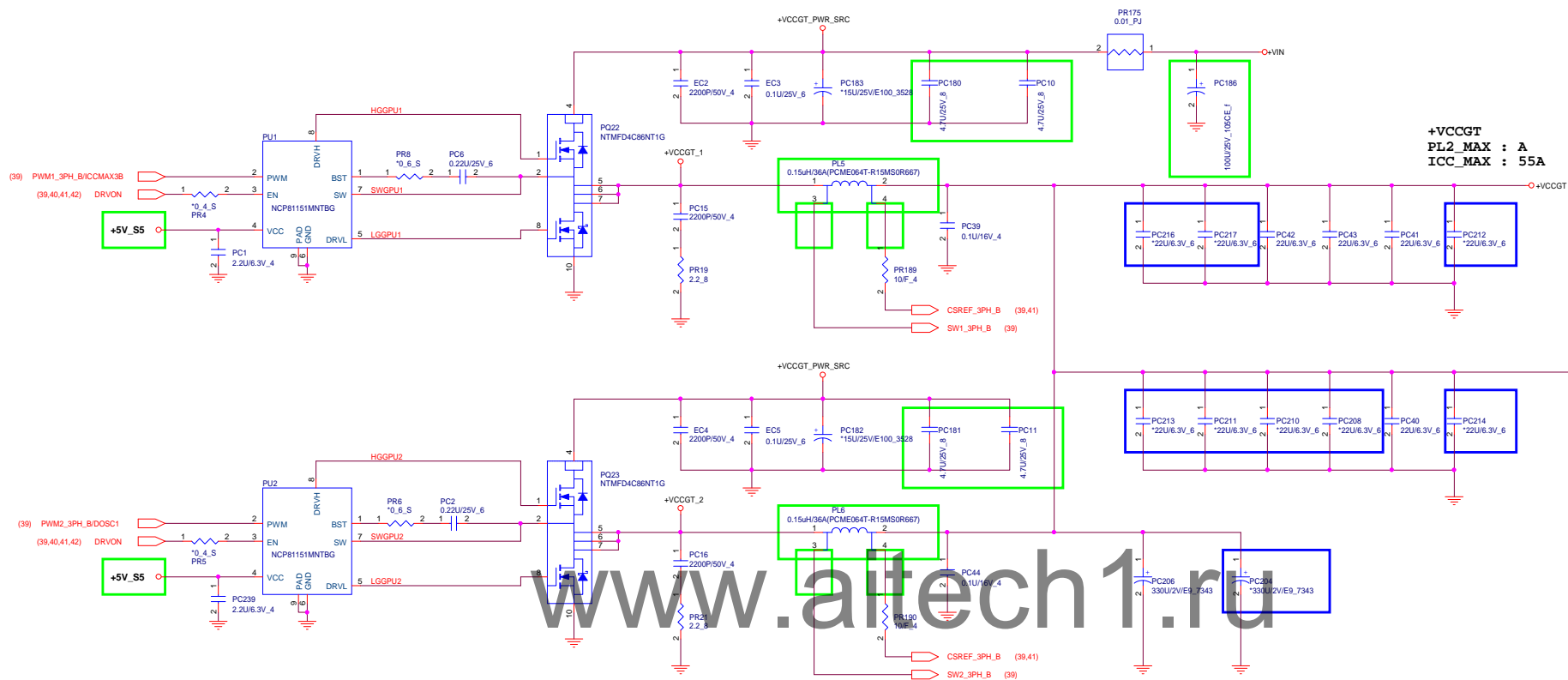


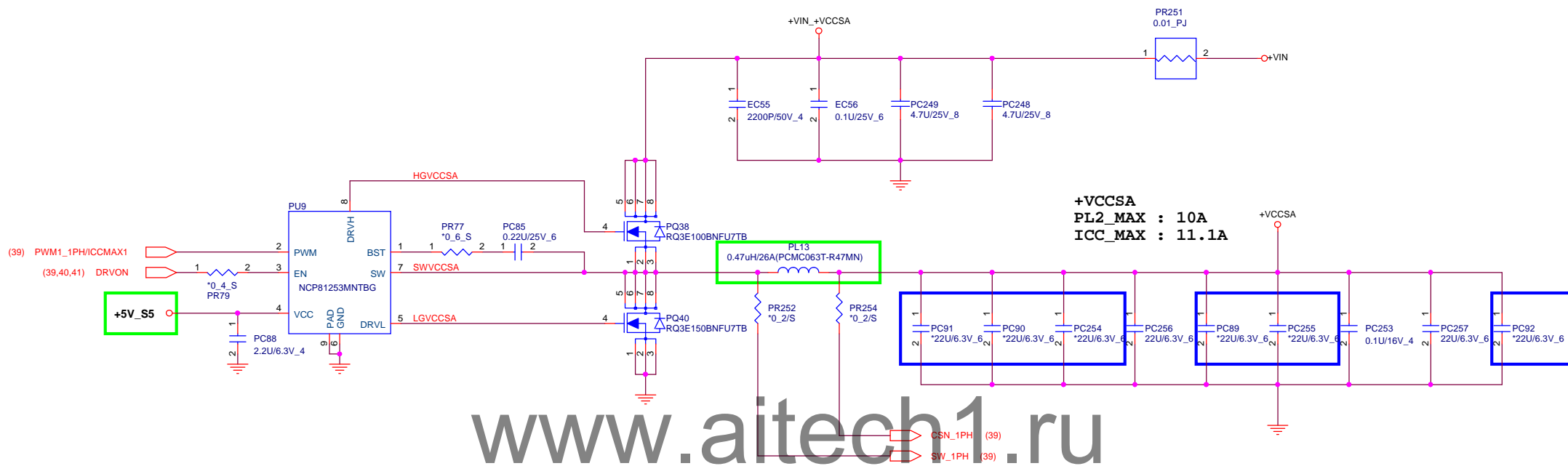
**PROJECT : NL8A**  
**Quanta Computer Inc.**

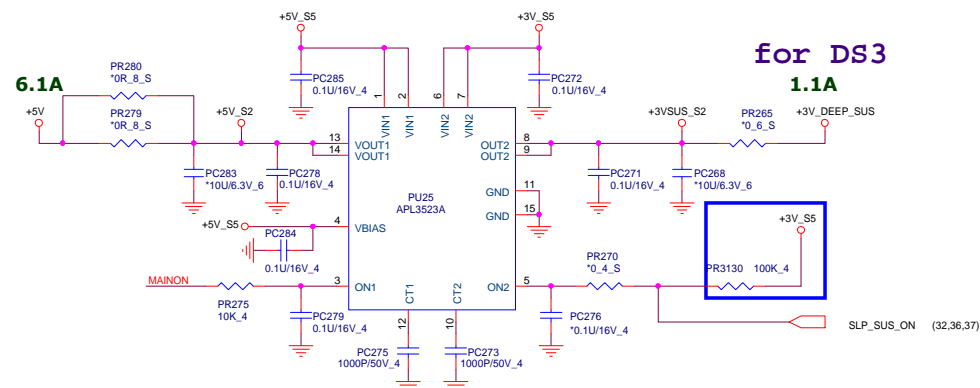
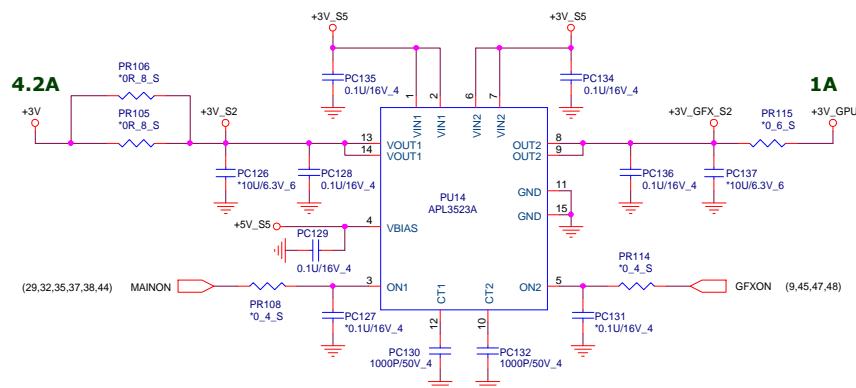
Size Custom	Document Number <b>+1.8V (APW8713)</b>	Rev 3B
Date: Wednesday, October 14, 2015	Sheet 38 of 61	







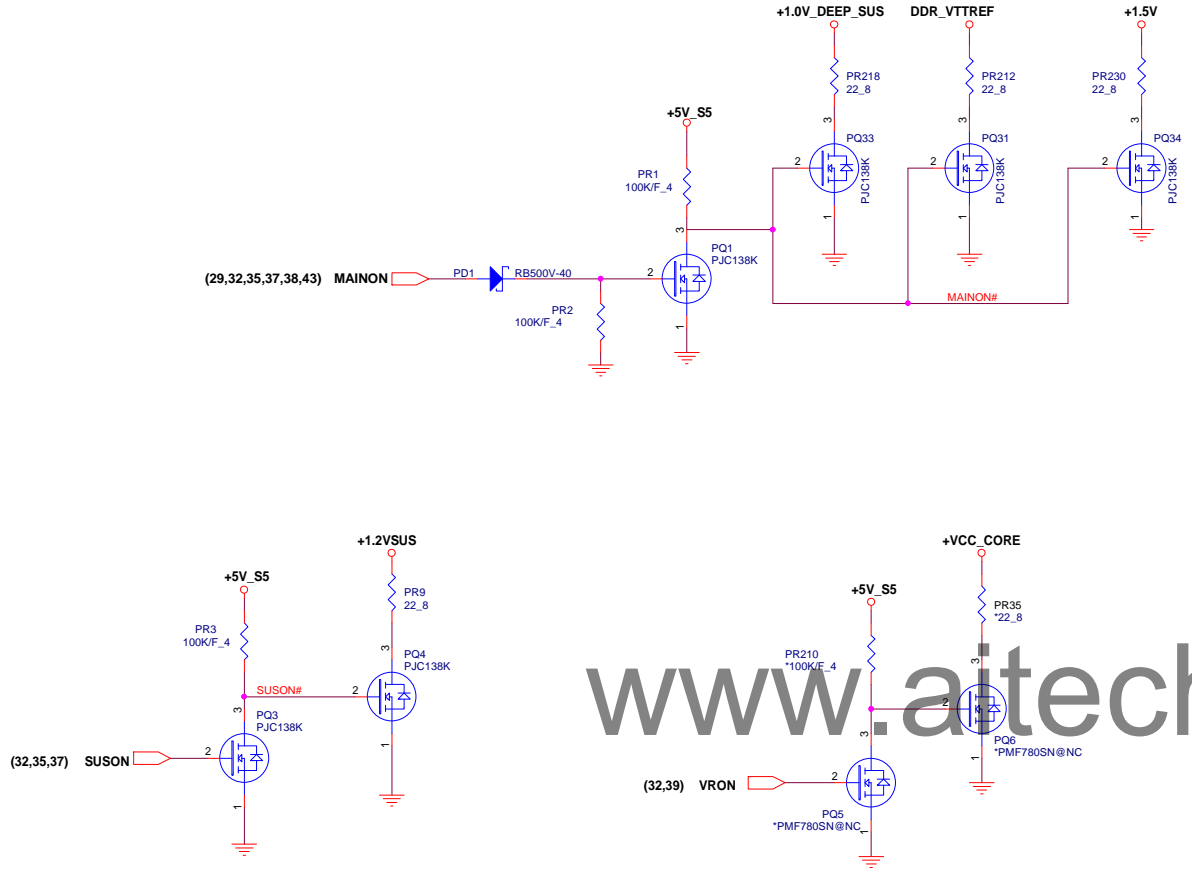




[www.aitech1.ru](http://www.aitech1.ru)

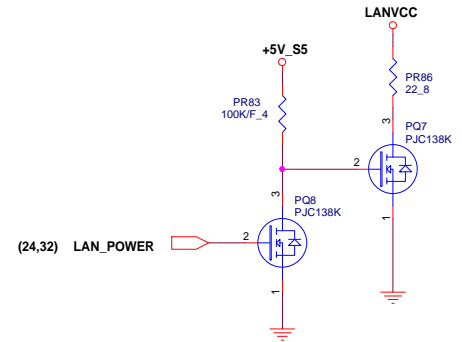
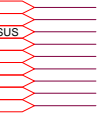


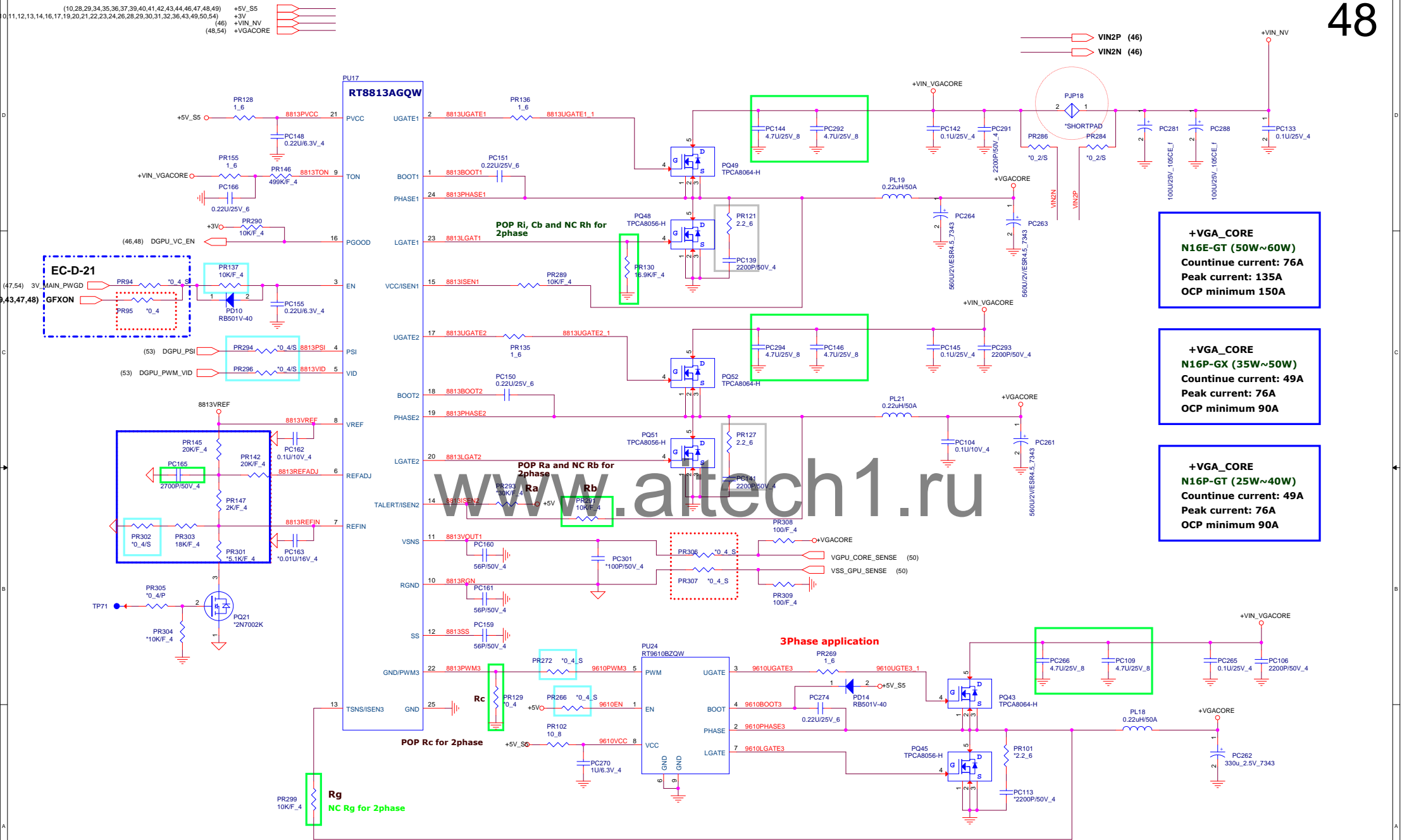
DISCHARGE

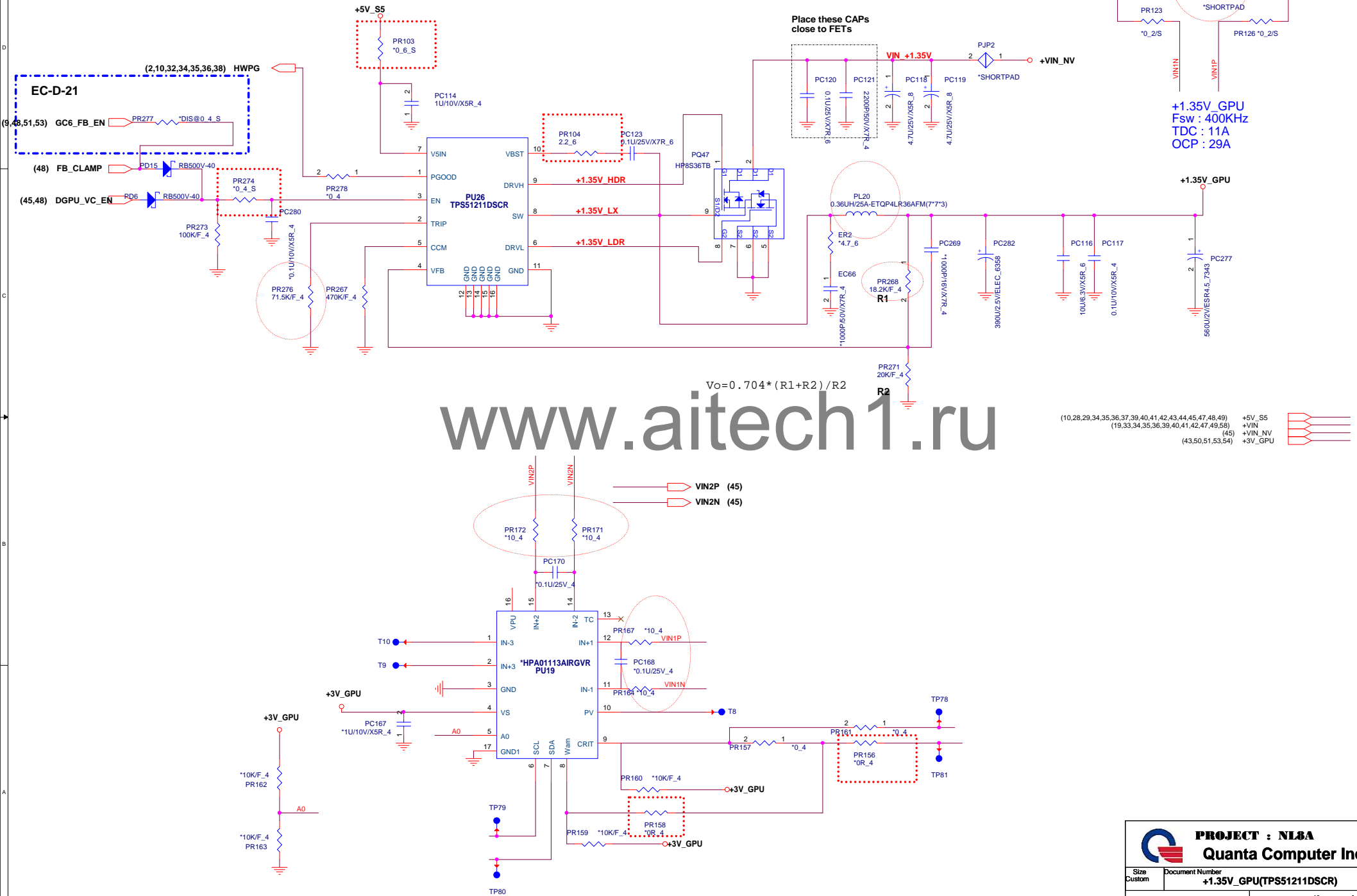


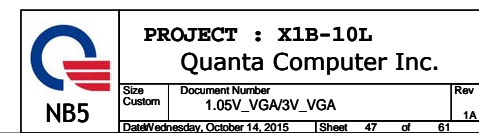
- (20,21,22,23,25,30,31,43,45,49,58)
- (9,10,11,12,13,14,16,17,19,20,21,22,23,24,26,28,29,30,31,32,36,43,45,49,50,54)
- (10,11,14,36,37,39)
- (16,17,35)
- (21,22,38)
- (2,6,10,16,17,35,47)
- (10,28,29,34,35,36,37,39,40,41,42,43,45,46,47,48,49)
- (7,40)
- (24)

- +5V
- +3V
- +1.0V\_DEEP\_SUS
- DDR\_VTTREF
- +1.5V
- +1.2VSUS
- +5V\_S5
- +VCC\_CORE
- LANVCC



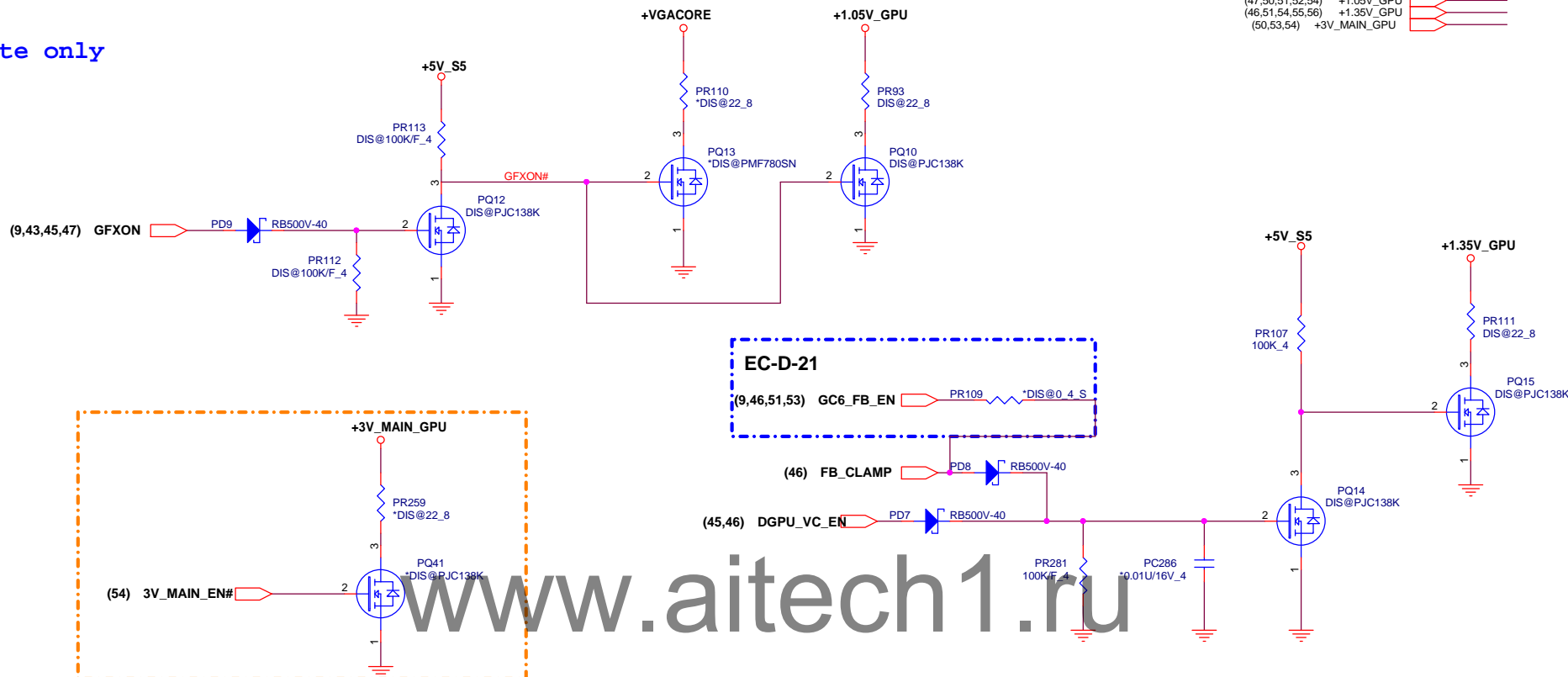






Discrete only

51



(43,46,50,51,53,54) +3V\_GPU  
(45,54) +VGACORE  
(47,50,51,52,54) +1.05V\_GPU  
(46,51,54,55,56) +1.35V\_GPU  
(50,53,54) +3V\_MAIN\_GPU

EC-D-21

(9,46,51,53) GC6\_FB\_EN PR109 \*DIS@0.4 S

(46) FB\_CLAMP PD8 RB500V-40

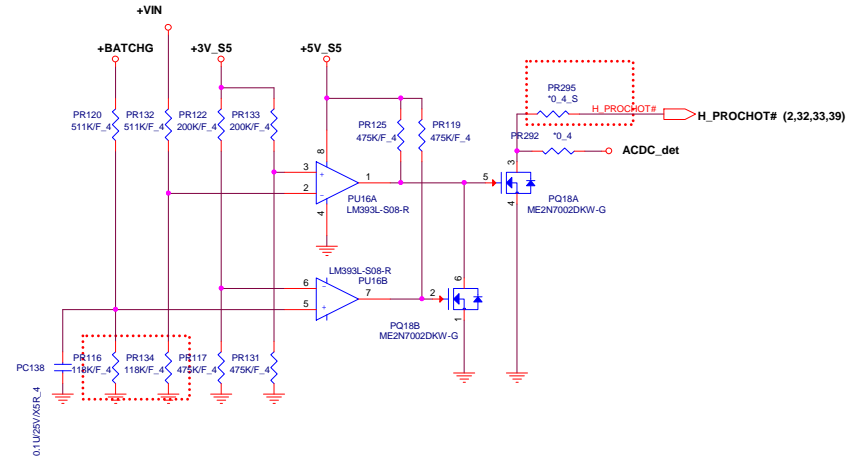
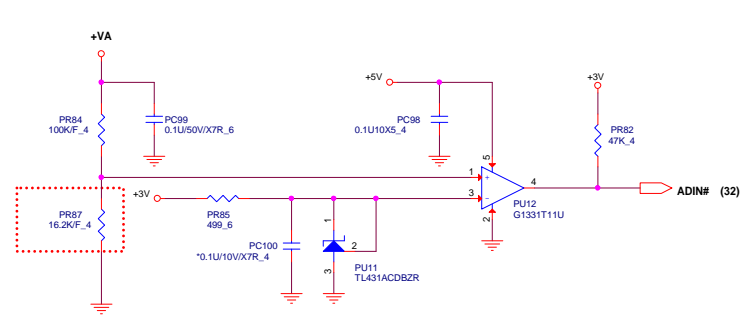
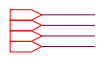
(45,46) DGPU\_VC\_EN PD7 RB500V-40

(54) 3V\_MAIN\_EN#



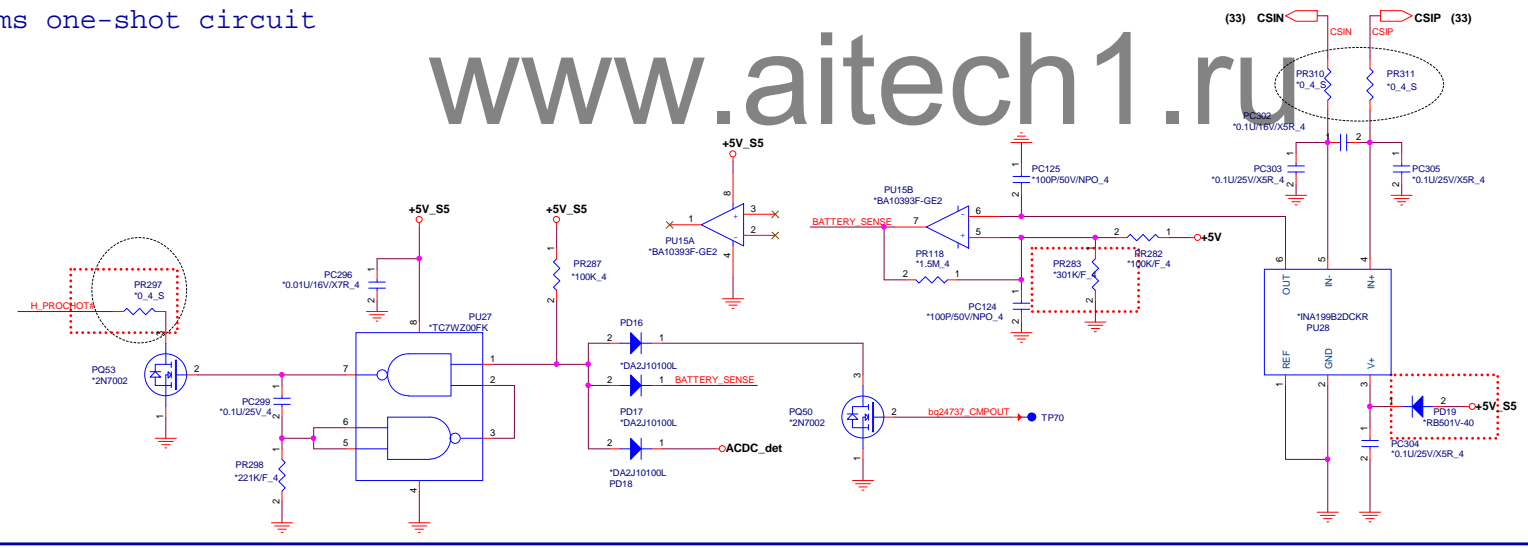
PROJECT : NL8A  
Quanta Computer Inc.

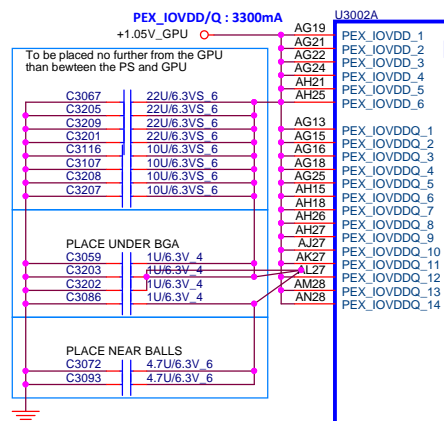
Size	Document Number	Rev
Custom	Discrete Discharge	3B
Date:	Wednesday, October 14, 2015	Sheet 48 of 61



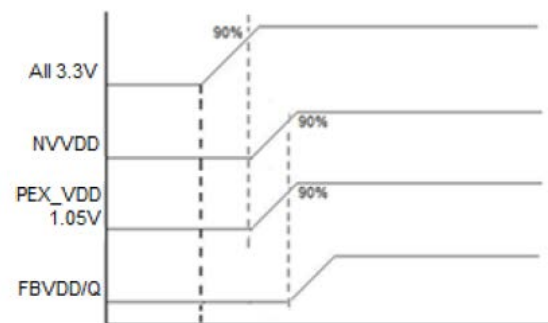
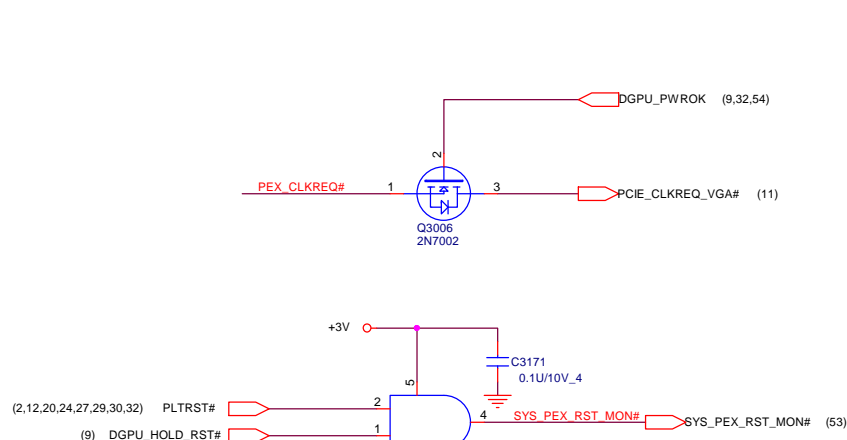
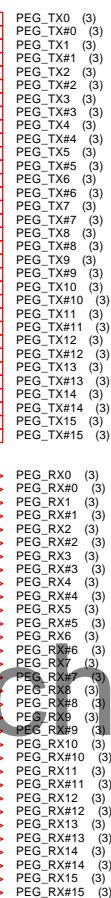
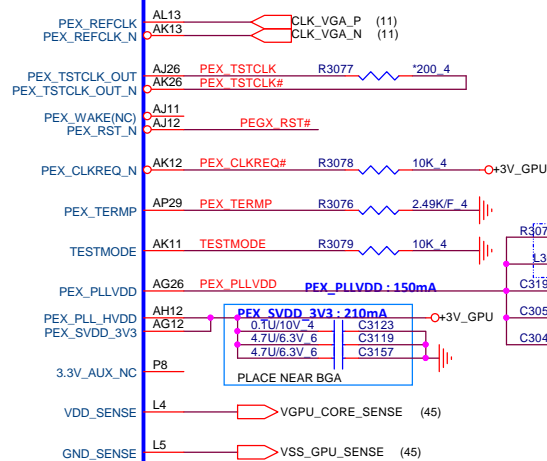
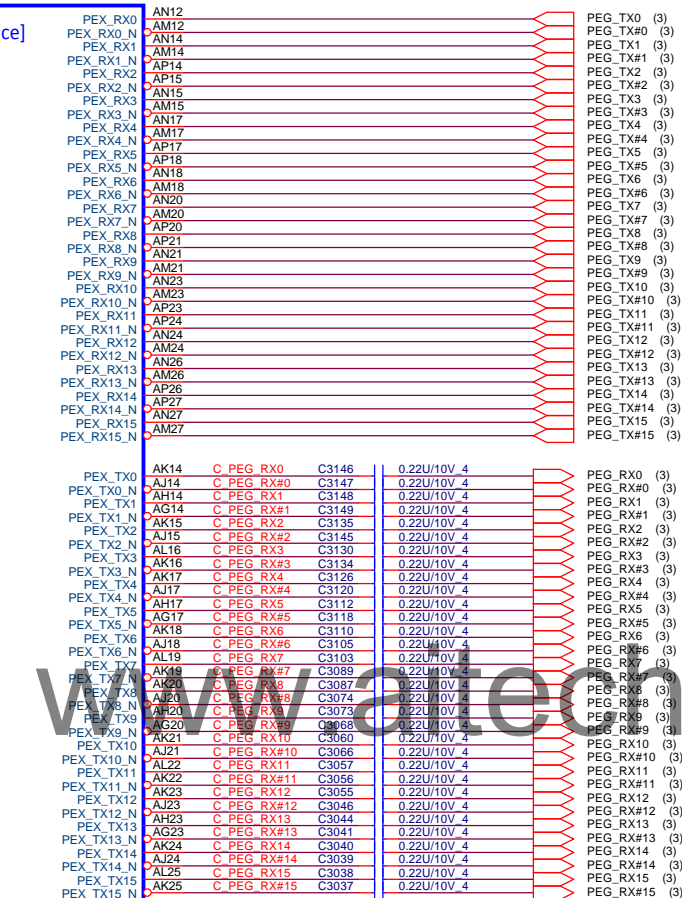
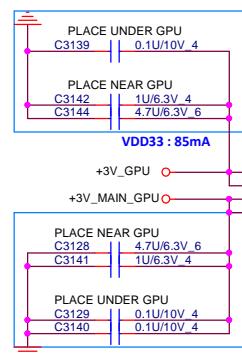
10ms one-shot circuit

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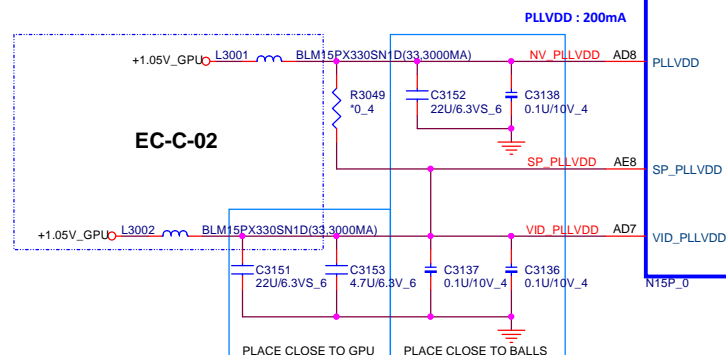
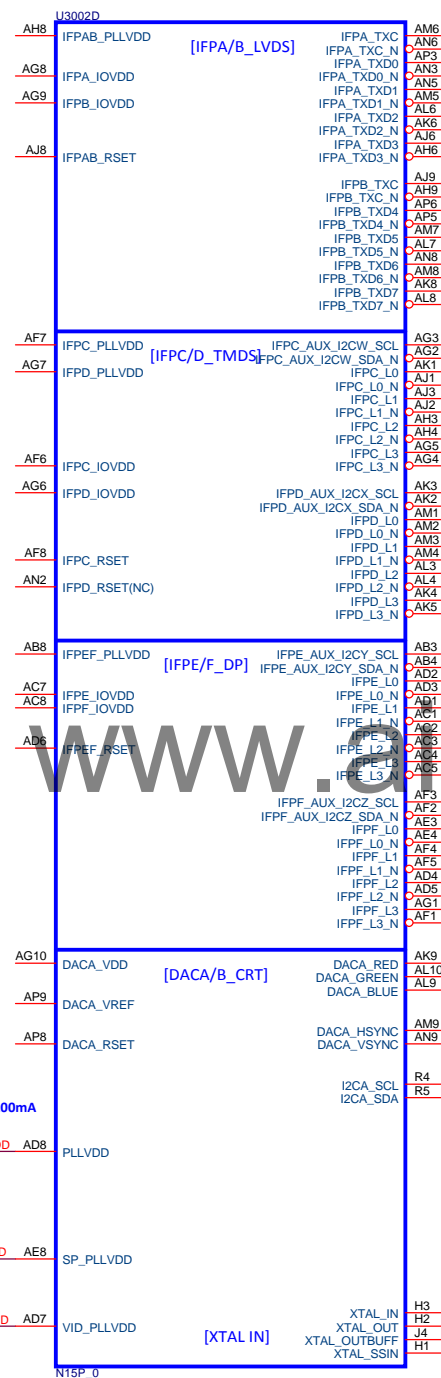
AC8 NC\_1  
AJ28 NC\_2  
AJ4 NC\_3  
AJ5 NC\_4  
AL11 NC\_5  
C15 NC\_6  
D19 NC\_7  
D20 NC\_8  
D23 NC\_9  
D28 NC\_10  
H31 NC\_11  
T8 NC\_12  
V32 NC\_13



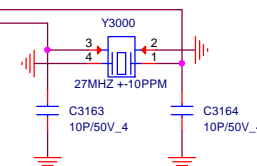
**PROJECT : NL9**  
**Quanta Computer Inc.**



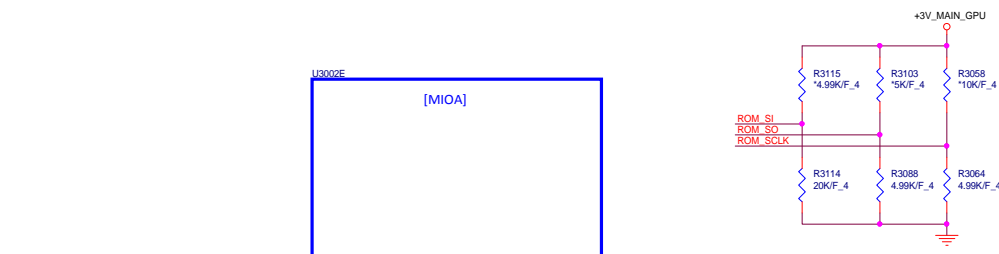




H3 VGA\_XTALIN  
H2 VGA\_XTALOUT  
J4 R3057 10K 4  
H1 R3094 10K 4



**PROJECT : NL9**  
**Quanta Computer Inc.**



Default: GDDR5 Hynix 2G VRAM (for NL8)

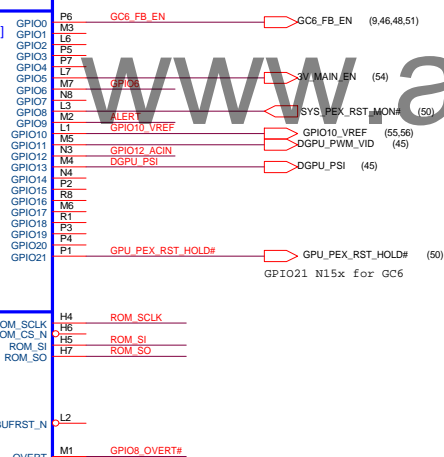
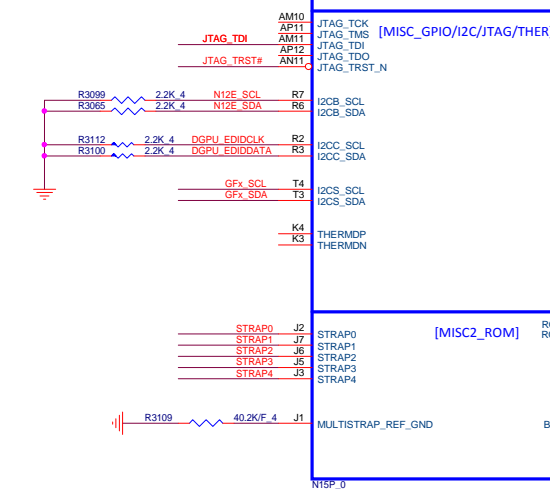
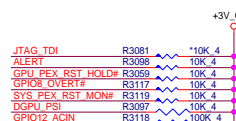
Memory Size	Vendor	P/N	Mfr. P/N	ROM_SI	
128M x 16	Samsung	AKG5MWDT502	X4G20325FD-FC03	0000 (0x0)	4.99K PD
256M x 16	Hynix (1.35V)	AKG5PWUTW11	H5GC4H24AJR-T2C	0110 (0x6)	34.8K PD
256M x 16	Samsung (1.35V)	AKG5PGDT500	X4G41325FC-HC03	0011 (0x3)	20K PD

Netname	
ROM_SO	4.99K PD
ROM_SCLK	4.99K PD
STRAP0	49.9K PU
STRAP1	
STRAP2	
STRAP3	
STRAP4	

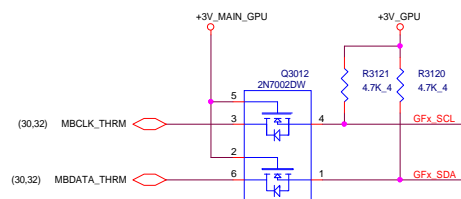
4.99K/F 4: CS24992FB26 RES CHIP 4.99K 1/16W +1% (0402)  
 10K/F 4: CS31002FB26 RES CHIP 10K 1/16W +1% (0402)  
 15K/F 4: CS31502FB24 RES CHIP 15K 1/16W +1% (0402)  
 20K/F 4: CS32002FB29 RES CHIP 20K 1/16W +1% (0402)  
 24.9K/F 4: CS32492FB16 RES CHIP 24.9K 1/16W +1% (0402)  
 30.1K/F 4: CS33012FB18 RES CHIP 30.1K 1/16W +1% (0402)  
 34.8K/F 4: CS33482FB22 RES CHIP 34.8K 1/16W +1% (0402)  
 45.3K/F 4: CS34532FB18 RES CHIP 45.3K 1/16W +1% (0402)

Logical Strap Bit Mapping

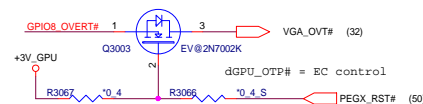
Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111



Gfx SMBus Isolation



GPIO8 VGA thmtrip# => inform EC over temperature protect



Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	PCL_DEV0[4]	SUB_VENDOR	PC_DEV0[5]	PEX_PLL_EH_TERM
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	FB[1]	FB[0]	SMBL_ALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	PCL_DEV0[3]	PCL_DEV0[2]	PCL_DEV0[1]	PCL_DEV0[0]
STRAP3	SOR2_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	PCIE_SPEED_CHAN	PCIE_SPEED_CHAN	PCIE_MAX_SPEED	DP_PLL_VDD33V

Table 9. H14P-GV/GT/GS/LP/GE GDDR5 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/V FBVDDQ	Manufacturer Part Number	Max Speed WCL (MHz)	Memory Data Code Minimum	Status
128Mx16 GDDR5	Hynix	0x1	1.5 V 1.5 V	H5GQ2H04AFR-T2C	2300	N/A	Production Candidate
		0x6	1.35V 1.35V	H5GQ2H04AFR-T2C	2000	N/A	Production Candidate
	Samsung	0x5	1.5 V 1.5 V	K4G20325FD-FC04	2500	1219	Production Candidate
		0x7	1.35V 1.35V	K4G20325FD-FC04	2000	1219	Production Candidate

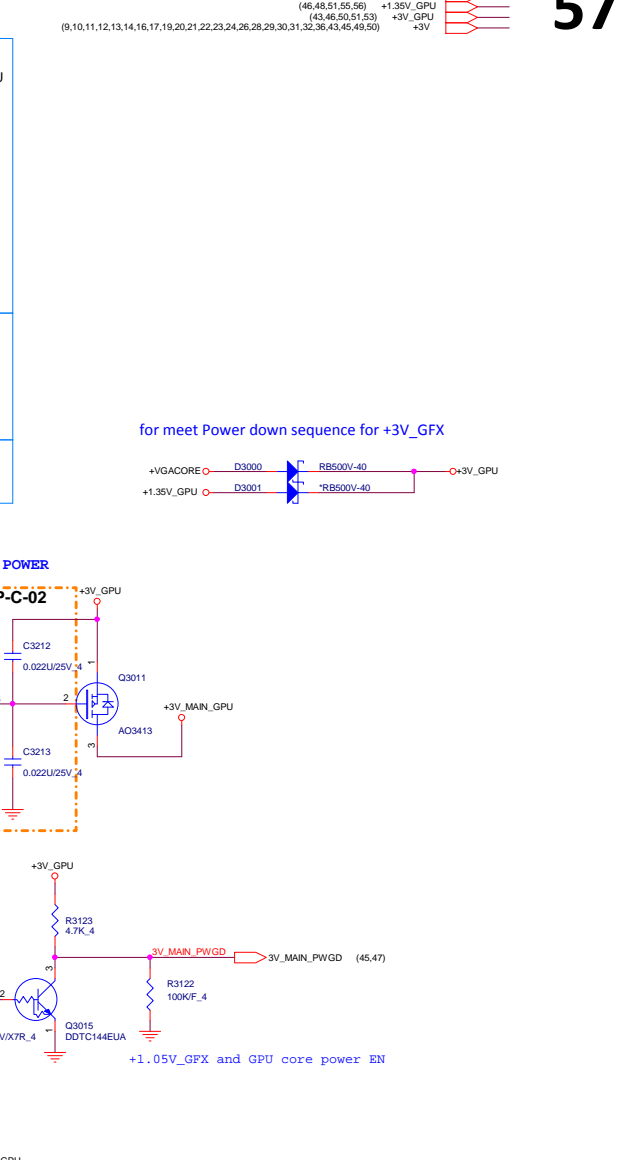
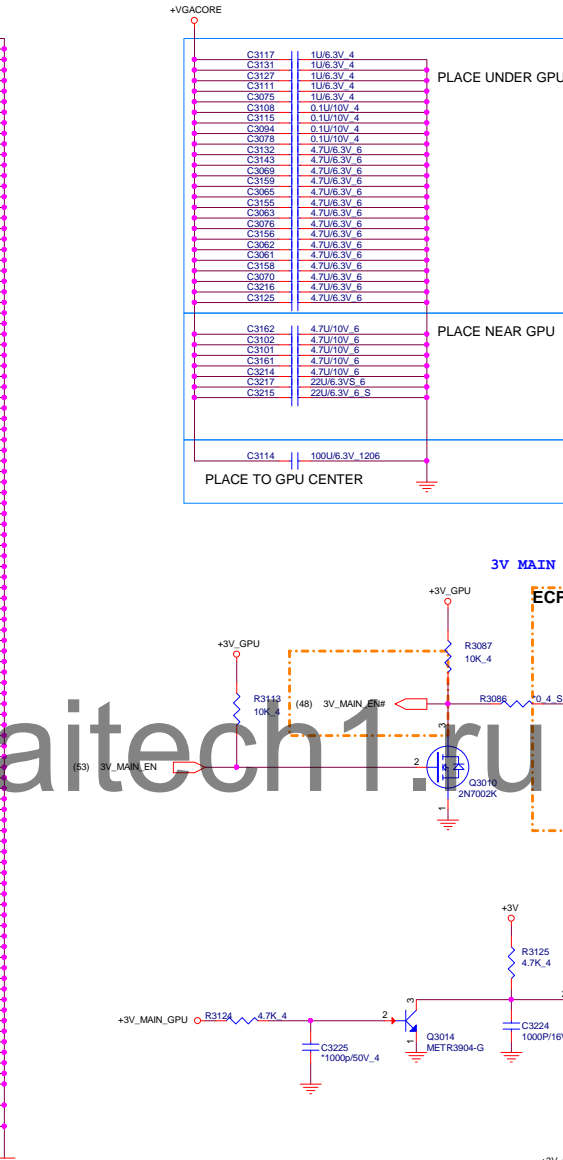
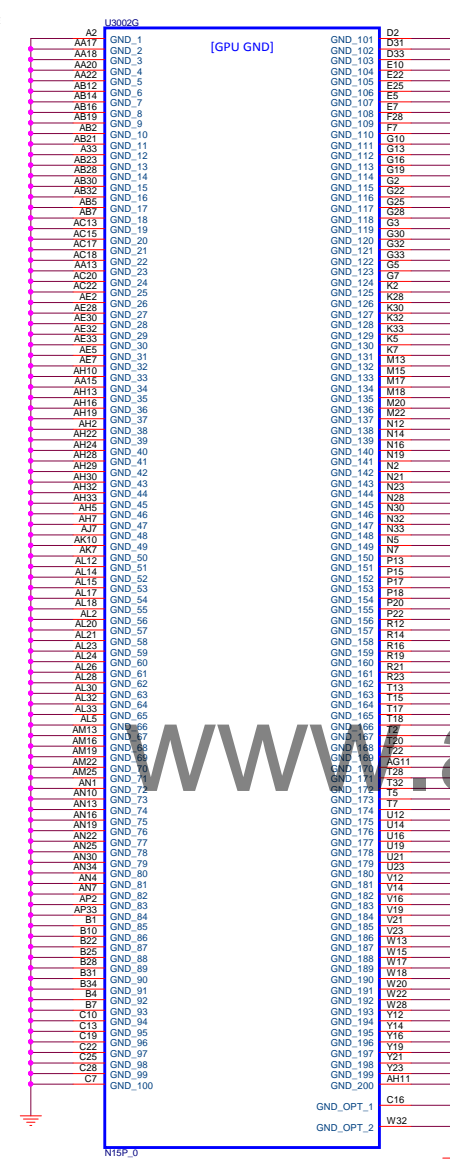
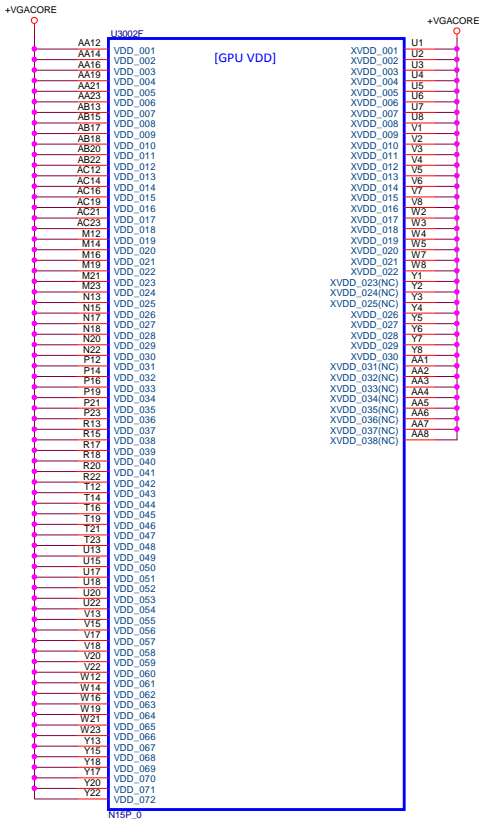
## GPIO ASSIGNMENTS

GPIO	Function
GPIO 0	Debug Service Header
GPIO 1	MEM_VDD_CTL/FAN_PWM
GPIO 2	LCD Brightness Control (BL_PWM)
GPIO 3	LCD Power Enable (PPEN)
GPIO 4	LCD Backlight Enable (BLEN)
GPIO 5	NVDD PWM_VID_BOOT_EN
GPIO 6	Remote Sensor Error Correction
GPIO 7	3D STEREO
GPIO 8	GPU Overtemp
GPIO 9	GPU Thermal Alert/FAN_PWM
GPIO 10	FB Vref Control
GPIO 11	NVDD PWM_VID
GPIO 12	PWR_Level AC Detect
GPIO 13	NVDD PSI
GPIO 14	FB_CLAMP_TGL_REG/HPD for IFP AB (not used)
GPIO 15	HPD for IFP C (DP)
GPIO 16	Fan PWM/MEM_VDD_CTL/NVDD PSI/FAN LOCK
GPIO 17	HPD for IFP D (eDP)
GPIO 18	HPD for IFP E (DP)
GPIO 19	HPD for IFP F (DP)
GPIO 20	<not used>
GPIO 21	<not used>



**PROJECT : NL8**  
**Quanta Computer Inc.**

VDD/XVDD : 25.72A



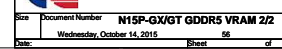
for meet Power down sequence for +3V\_GFX



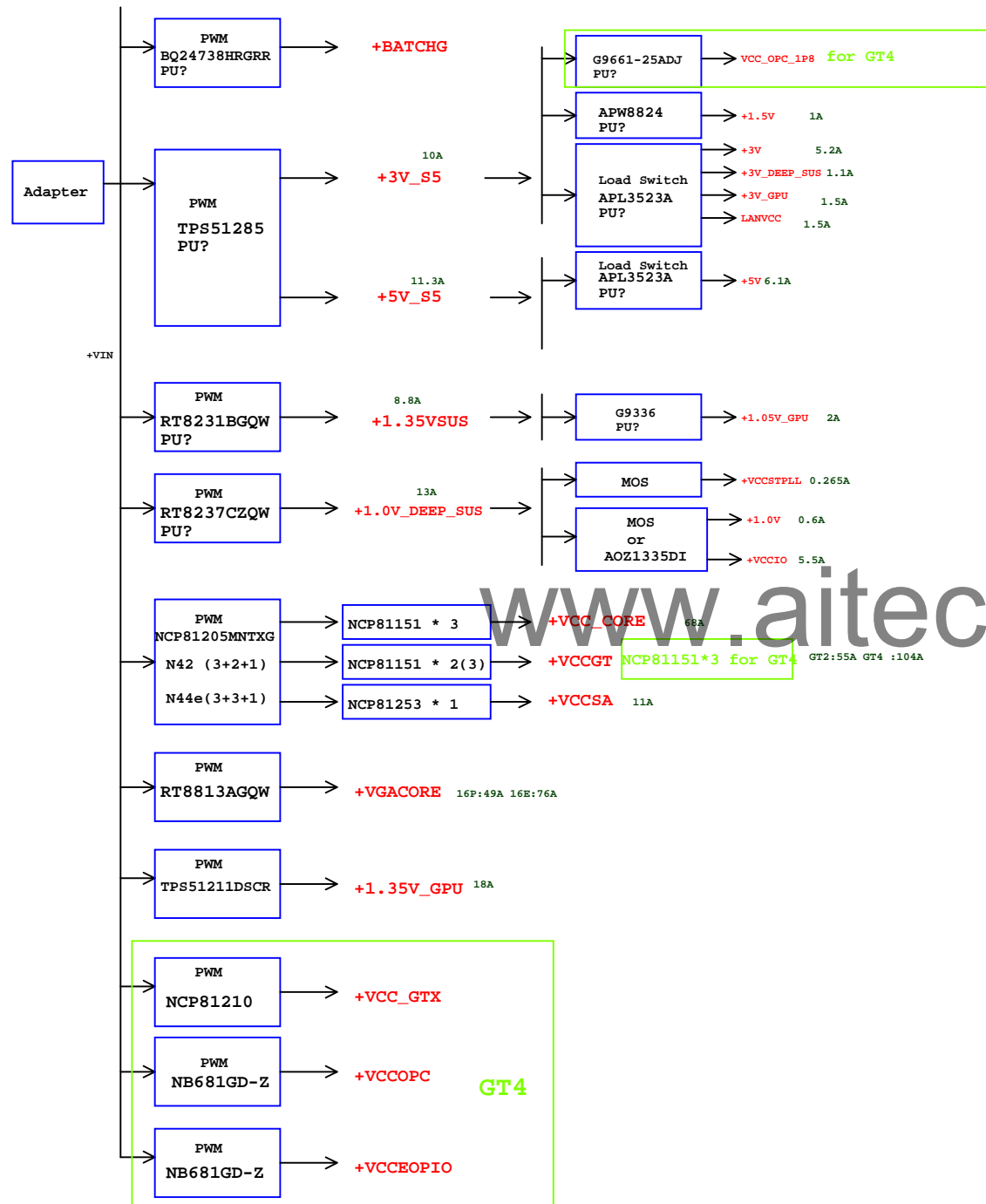
www.aitech1.ru

(45,48) +VGACORE  
(47,48,50,51,52) +1.05V\_GPU  
(46,48,51,55,56) +1.35V\_GPU  
(43,46,50,51,53) +3V\_GPU  
+3V



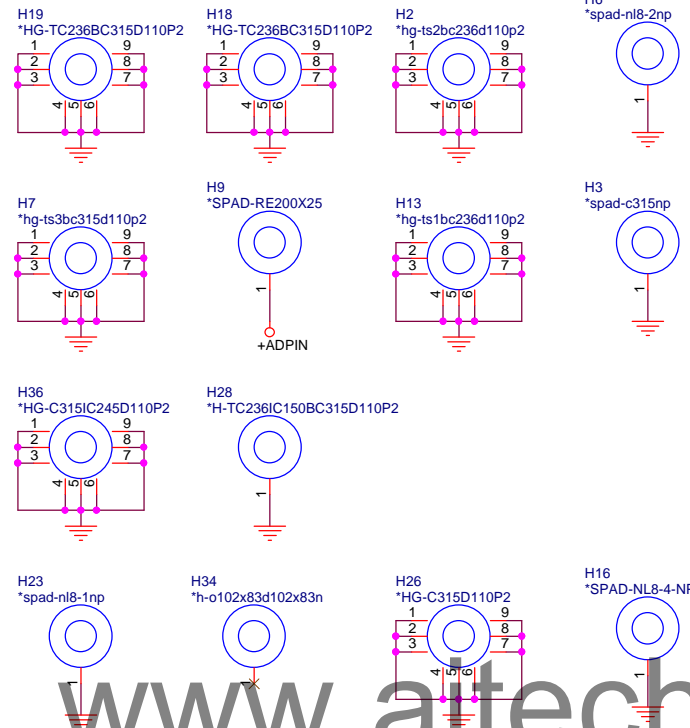
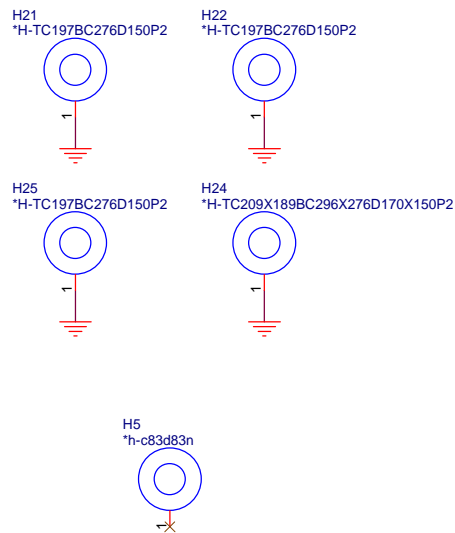


# Power Delivery Map

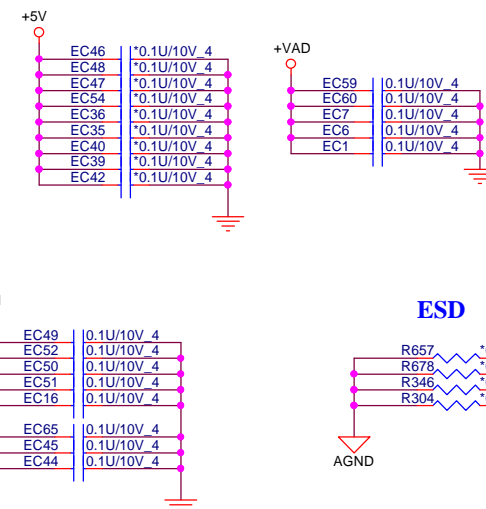




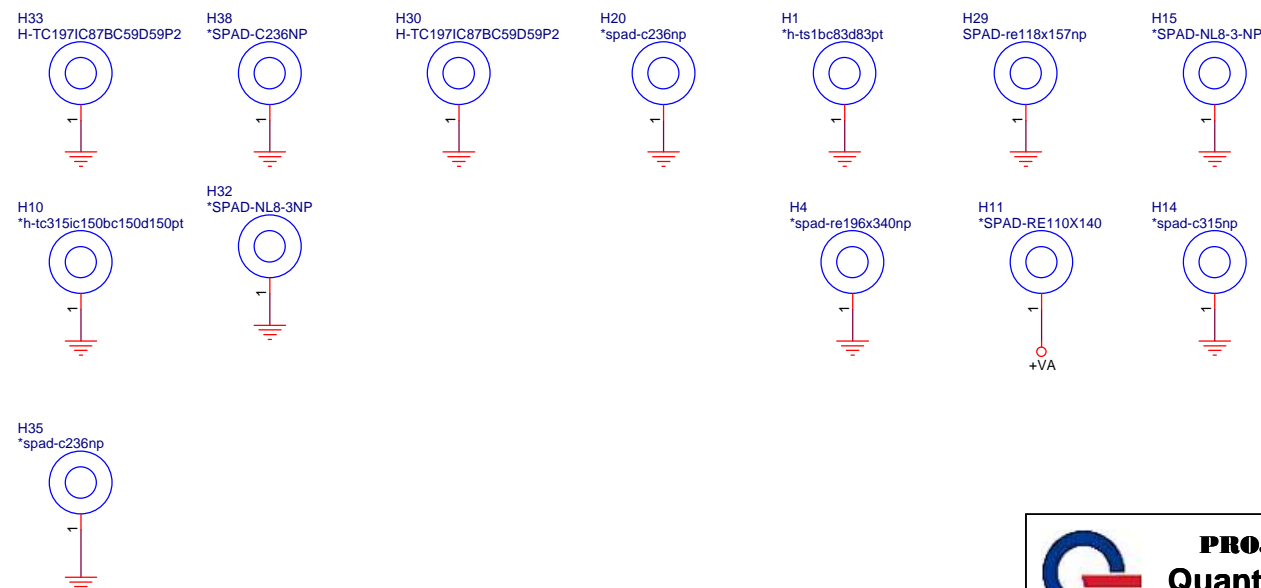
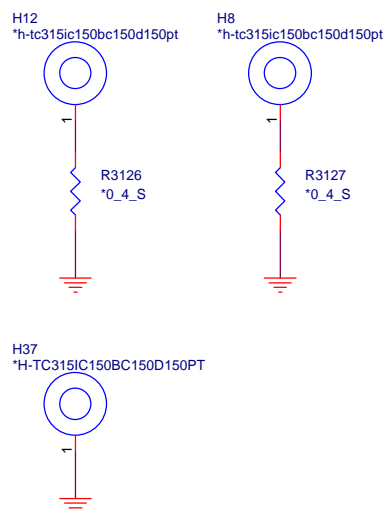
## CPU BRACKET



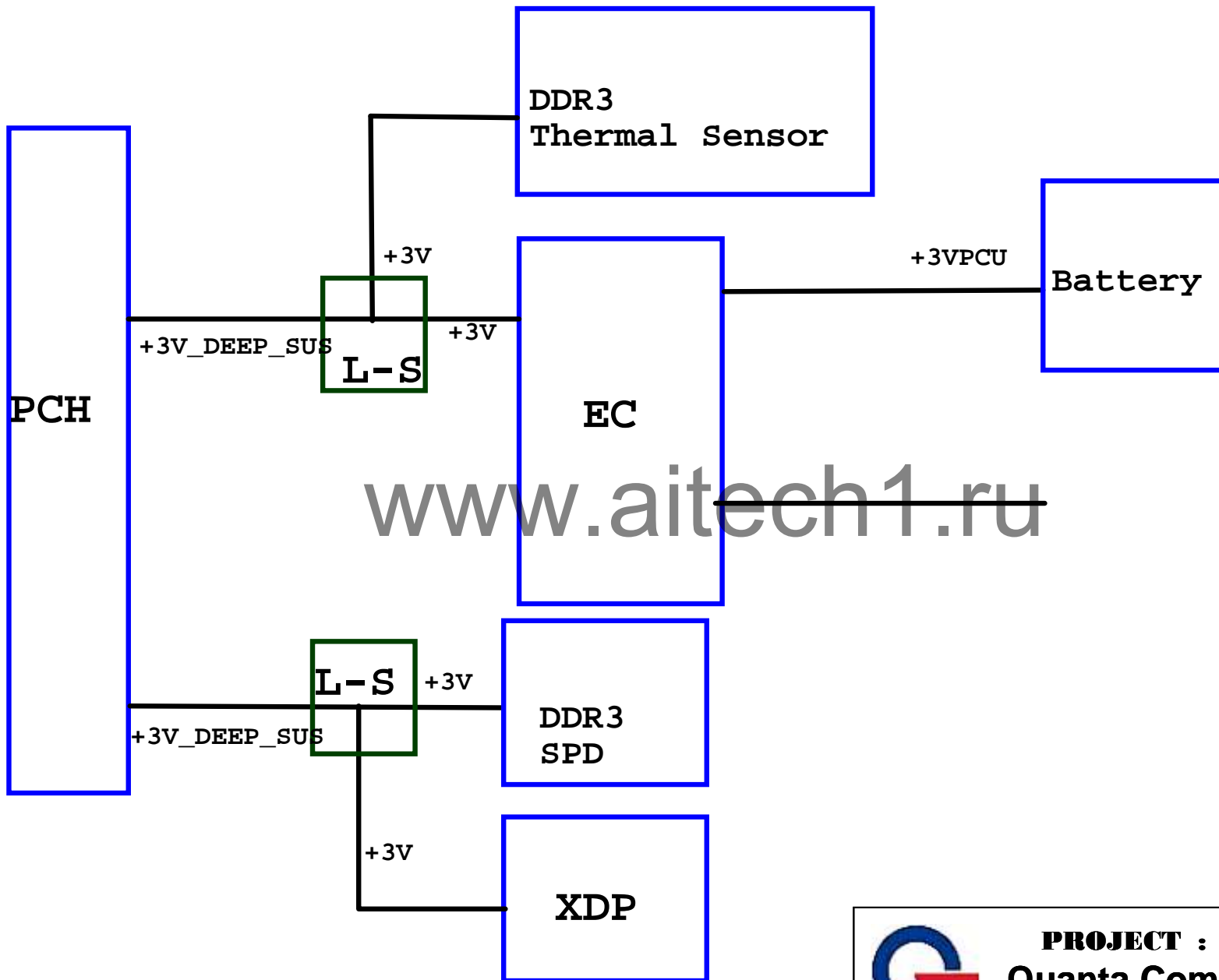
## EMI



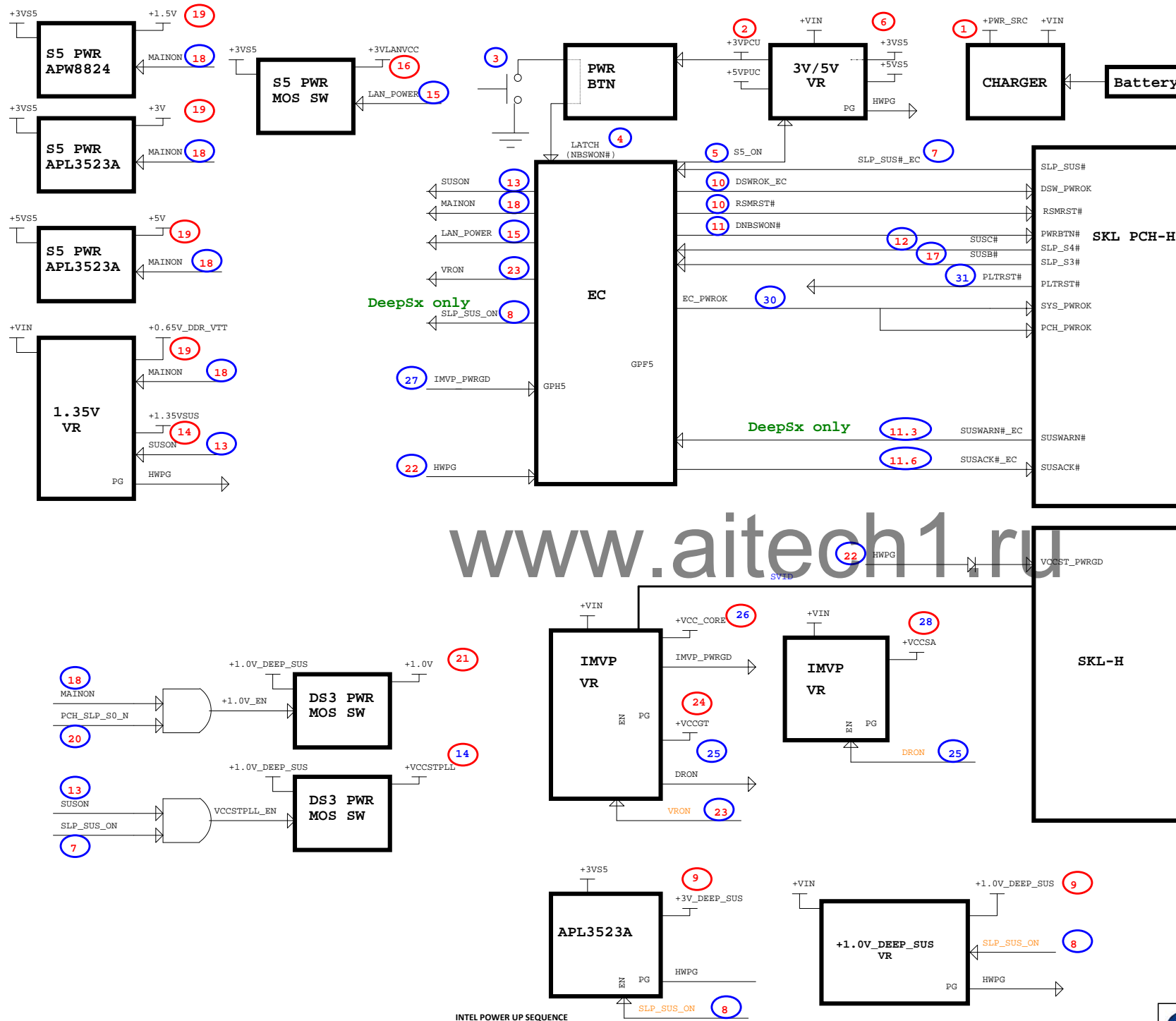
## VGA BRACKET











2015	EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
	SDV				
	EC-A-01	32	7/30	L3004 C3226	reserve N16E-GR power rail
	EC-A-02	11,25	8/12		SATA port4 change to port3 for HM170
	EC-A-03				N16E only
	EC-A-04	3,19	8/14	C45,c46,c47,c48	reserve for UHD panel
	EC-A-05		8/24		0ohm change to shortpad
	EC-A-06	30	8/26	Q51,Q35,Q33,Q34,U12,C617,C625,C626,R312,R313,R318,R325,R323,R322	ASM GPU thermal HW protect
SIT	EC-C-01	8	9/30		A36,A37 pin contact GND
	EC-C-02		9/30	L3000,L3001,L3002,L3003,L3004	EOD,change to CX5PX330000/CX330T30000 RC0402
	EC-C-03	24	9/30	C756,C757	change to 10p for crystal report
	ECP-C-01	50	10/12	PC110	change to 0.01u for GC6
	EC-C-05	30	10/08	R3129,R3130,R3131,R3132,Q57,Q58 (All no ASM)	Thermal request
	EC-C-06		10/12	C3212,C3213	ASM for GC6
	ECP-C-02	50	10/14	PQ44,PQ46,PR262,PR263,PR264(All ASM)	for UVP